ME141B Introduction to MEMS
November 1st, 2010
Example Homework #2

Problem 1:
We intend to use KOH etching to form a diaphragm on a (100) silicon wafer. It wil be a square membrane with a thickness well-defined by an etch stop (e.g., electrochemical etch stop of an SOI wafer), such that there are no real thickness variations in the diaphragm itself. What feature size is required to produce a square diaphragm with a 400 mm side length by 20 mm thickness on a silicon wafer that is 500 mm thick (this wafer thickness includes the membrane thickness)? What is the edge length variation of the diaphragm if the etch mask is misaligned 1 degree to the <110> directin? Assuming the sensitivity of a pressure sensor varies as the inverse fourth power of the diaphragm edge length, what percentage of variation can be attributed to mask misalignment?

Problem 1 Solution:
The figure shows the desired diaphragm features on a (100) silicon wafer. The mask feature size a can be expressed as a function of wafer thickness t_w, diaphragm thickness t_d, diaphragm dimension d and the intersection angle θ between {111} and {100} planes:

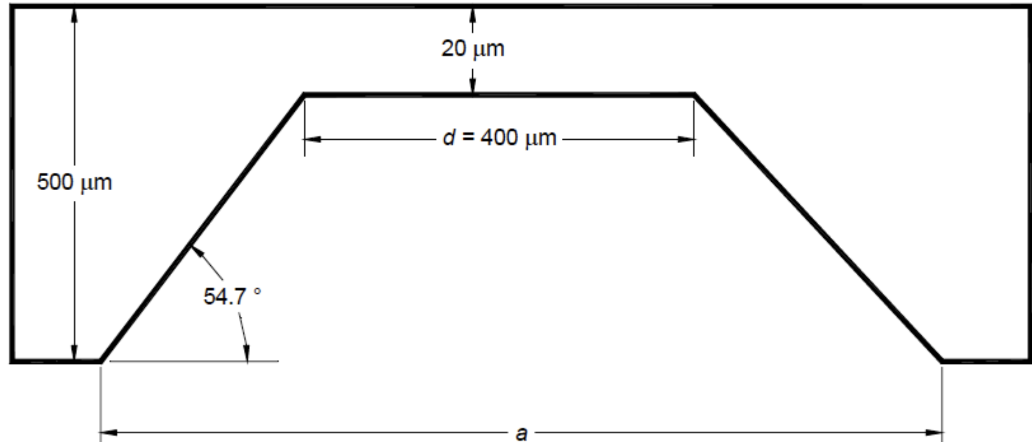
$$a = d + 2(t_w - t_d)\cot\theta$$

Substituting the numbers, we get a = 1079.7 um.

If the pattern is misaligned by θ= 1°, the actual size of the KOH pit will be (cos θ+ sin θ) and hence the edge length variation will be:

$$\Delta a = a(\cos\theta + \sin\theta - 1) = 18.7\ \mu m$$

This in turn translates to the edge-length variation for the diaphragm Δ d .



If the sensitivity S of a pressure sensor varies as the inverse fourth power of the diaphragm edge length d, i.e.

$$S \propto d^{-4}$$

then the percentage variation attributed to variations in wafer thickness is:

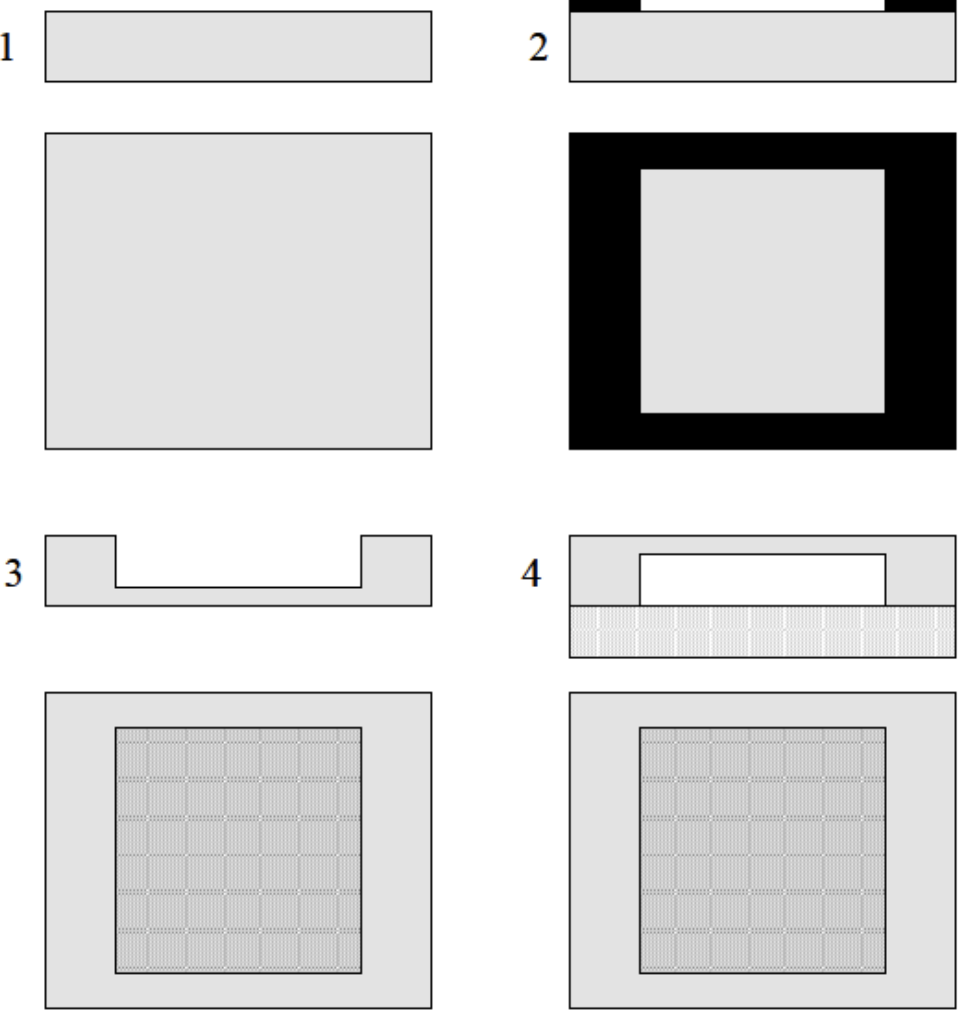
$$\% \frac{\Delta S}{S} \propto 4d^{-1} \cdot \Delta d \cdot 100\%$$
$$= 18.7\%$$

Problem 2: Debug and recreate a process and mask set for a pressure-sensing silicon diaphragm

You are a young junior faculty member who has just hired your first graduate student, Wayford Roppar. You have developed an idea for using a sealed-cavity pressure-sensing silicon diaphragm (1 mm across and 15 μm thick) that you're sure will make you famous and assure your tenure. You ask Wayford to design a process flow for creating this simple structure, and Wayford returns with the process flow detailed in Figure 1.

Being a seasoned MEMS designer, you immediately notice several critical errors with Wayford's process (things that won't work or won't produce the result that Wayford shows in the cross sections). Please find the critical errors in this process flow and, where possible, suggest alternate approaches. Do not worry about the accumulation of errors, but rather treat each step assuming that the structure up to that step could be created.

Then recreate a correct process flow along with the device cross sections at each step and the associated mask set (with dimensions).



Process steps:

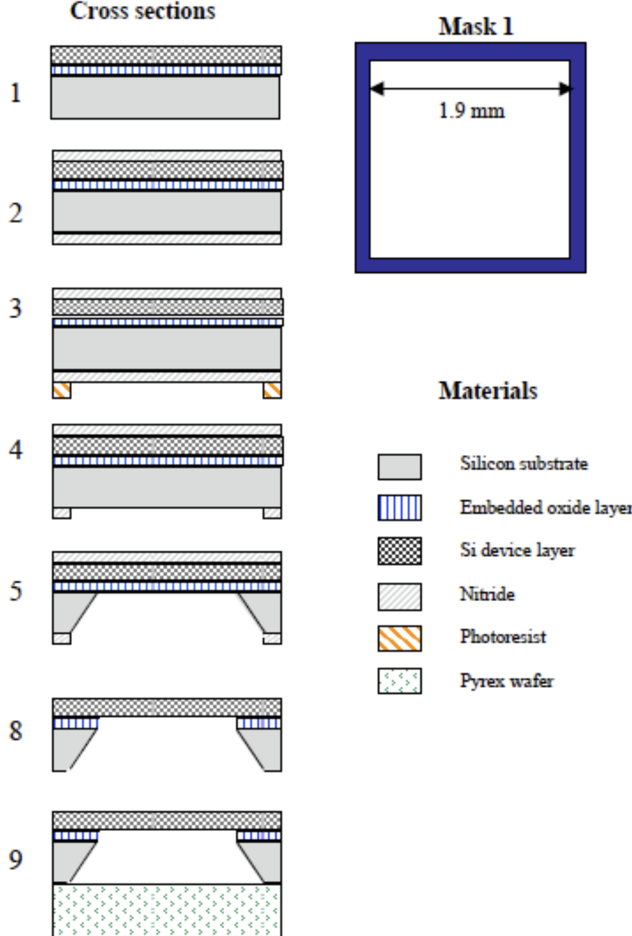
1. Start with a double-side-polished n-type silicon wafer.
2. Perform photolithography using 1-μm-thick positive photoresist to define the diaphragm area.
3. Deep-reactive-ion etch the silicon to form the diaphragm; ash resist.
4. Anodically bond the silicon wafer to a pyrex wafer.

Problem 2 Solution:

Proposed Process Step	Error
1. Start with a double side polished n-type silicon wafer	None yet!
2. Perform photolithography using 1-μm-thick positive photoresist to define the diaphragm area	Must precede with a clean (RCA or piranha)
3. Deep-reactive-ion etch the silicon to form the diaphragm; ash resist.	1 μm of PR is very thin when used as a mask in DRIE. In other words, since the selectivity of DRIE to silicon over PR is ~ 50:1, etching though ~ 500μm of Si would require more than 10μm of PR. Also, DRIE would lead to a non-uniform membrane thickness with variations on the order of the required thickness (15 μm). This will make the device function improperly if fabricated at all.
4. Anodically bond the silicon wafer to a pyrex wafer	Must precede with cleaning wafer

Corrected process:

1. Start with double-side polished SOI wafer, device layer 15 μm thick, oxide layer 1μm thick, substrate 500 μm thick. RCA clean.
2. Deposit LPCVD nitride, 0.5 μm thick (will coat both sides).
3. Spin 1-μm-thick positive photoresist on bottom side and perform photolithography using Mask 1 to the bottom side.
4. Dry etch the nitride on the bottom side using CF_4 /H_2 plasma for example. Ash resist .
5. KOH etch the silicon from the bottom side using the embedded oxide layer as an etch stop. If the dimensions of Mask 1 were calculated correctly, the resultant profile on the top side must be 1 mm across.
6. Piranha clean to remove all resist residue.
7. Etch the remaining nitride in 85% phosphoric acid.
8. Etch the exposed oxide using BOE for ~10 minutes. RCA clean.
9. Anodically bond the patterned SOI wafer to a Pyrex wafer.



Cross sections
1
2
3
4
5
8
9
Mask 1
1.9 mm
Materials
Silicon substrate
Embedded oxide layer
Si device layer
Nitride
Photoresist
Pyrex wafer

Problem 3:

The figure below shows an electrical trap that uses dielectrophoresis (DEP) to trap cells. You will design a process and mask set that will produce this structure (not to scale). Both metal layers must be 0.5-µm-thick gold (though other metals are acceptable beneath the gold). The substrate B and layer A both must be electrical insulators. The gold linewidth is 10 µm, and all other critical parameters are specified in the figure.

You are asked to create a table of process steps, along with process flow cross-sectional diagrams and masks. Specify materials and the proposed etch methods, and be sure to include as steps in your process the required wafer cleans, application of photoresist, and stripping of photoresist. You do not need to include dimensions in your mask set in this problem (but do draw the geometries correspondingly).

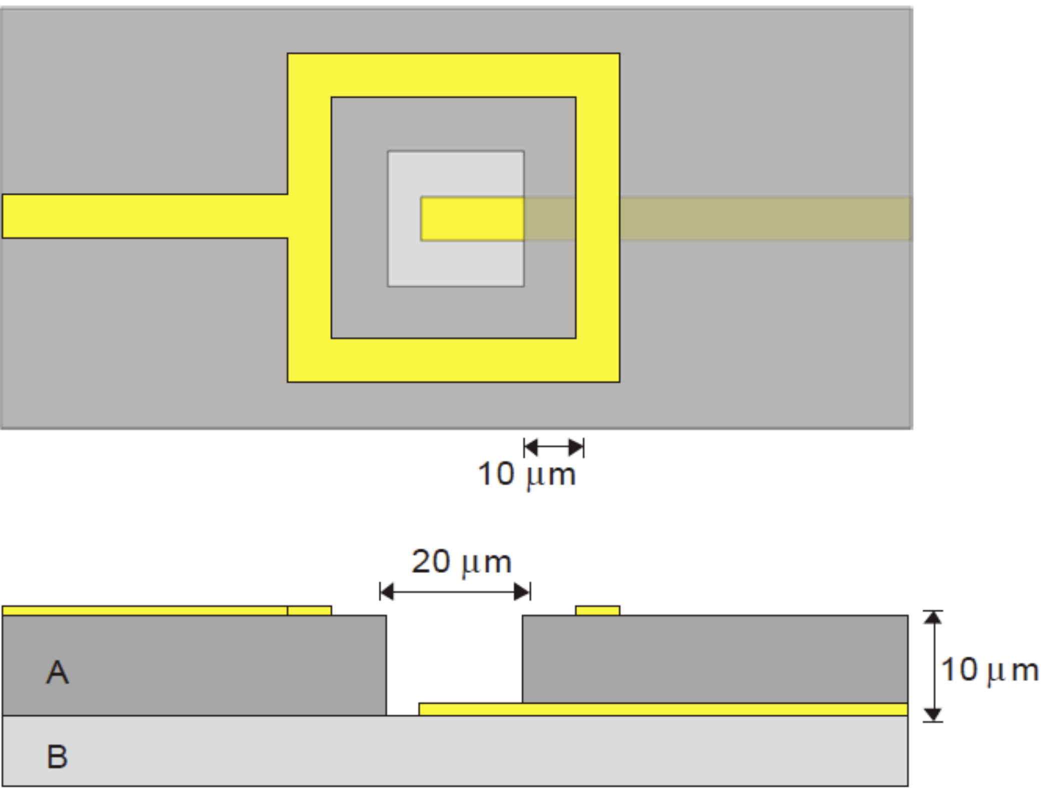


Figure 2. Schematic of a DEP trap (not to scale)

Problem 3 solution:

Step		Description
Starting Material: Glass Wafer		4” or 6” will be used as insulating layer B
1	Clean	Piranha or RCA1, solvent clean would be acceptable
2	Photolithography	Using negative resist and Mask 1. Thickness of resist at least 1.5 µm (3 times that of the layer to be lifted off). Negative resist necessary for lift off process later on
3	Deposit Au-Ti bilayer	E-beam evaporation (good for lift-off to be performed in next step). thickness of gold ~ 0.5 µm, thickness of titanium ~ 100 Å. Ti used as adhesion layer.
4	Lift-off Au-Ti bilayer	Acetone. Followed by water rinse.
5	Clean	Solvent clean good here – Pirahna may eat up some of the Ti layer and may lead to delamination of gold layer
6	Deposit Silicon Oxide	PECVD, about 10 µm thickness. Will be used as insulating layer A.
7	Photolithography	Use negative resist and Mask 2. Thickness of resist must be greater than 1.5 um.
8	Deposit Au-Ti bilayer	E-beam evaporation. Thickness of gold ~ 0.5 µm, thickness of titanium ~ 100 Å. Ti used as adhesion layer.
9	Lift-off Au-Ti bilayer	Acetone. Followed by solvent clean and water rinse.
10	Photolithography	Spin cast positive thick photoresist, prebake; expose MASK 3, develop, postbake
11	Etch Oxide	Dry etch using CF4/H2 plasma. Anisotropic and selective over Si.
12	Strip Resist	Ash with an Asher
13	Clean	Solvent clean ok.

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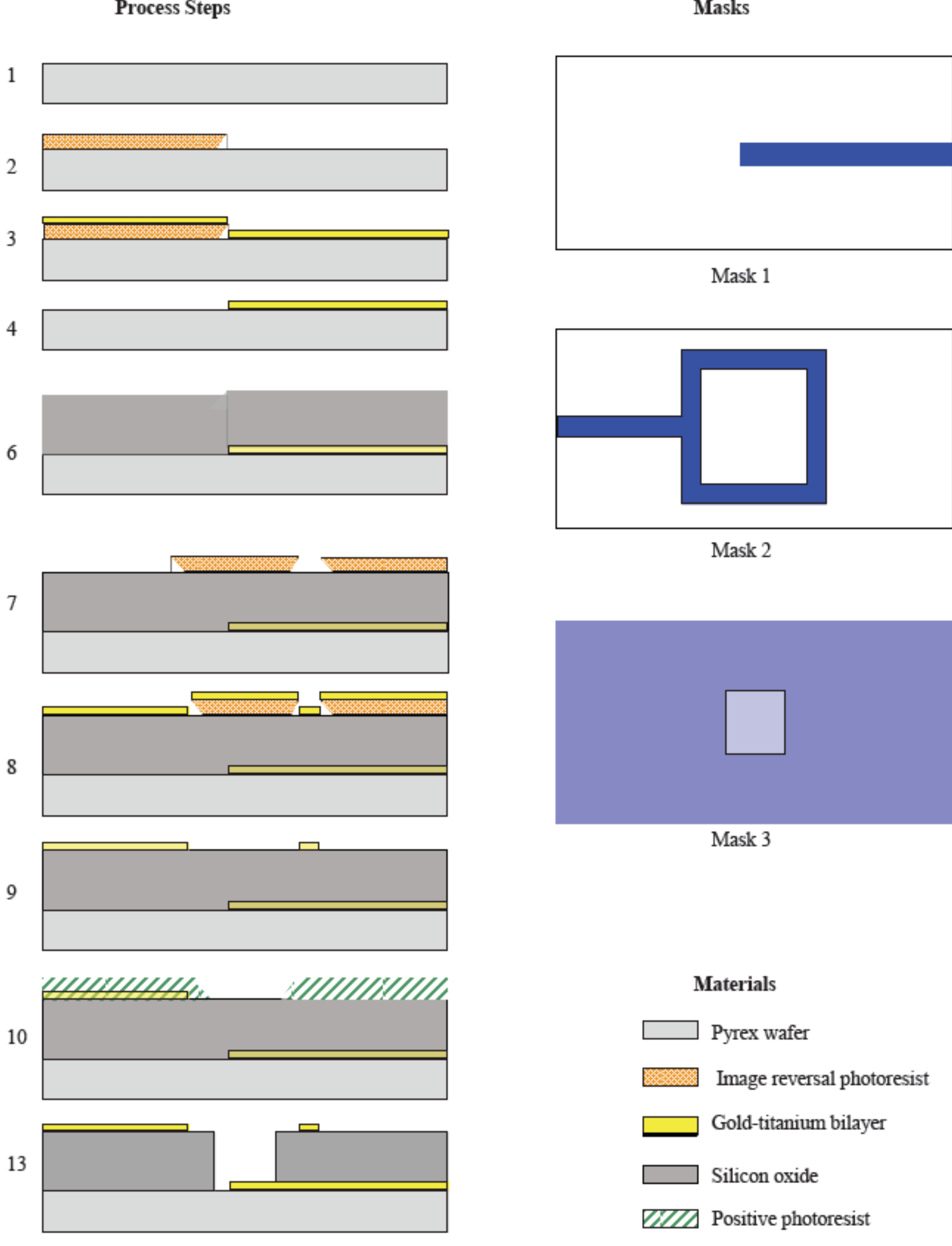
Process Steps
Masks
1
2
3
4
6
7
8
9
10
13
Mask 1
Mask 2
Mask 3
Materials
Pyrex wafer
Image reversal photoresist
Gold-titanium bilayer
Silicon oxide
Positive photoresist