ME141B: Introduction to MEMS
TAKE-HOME MIDTERM
DUE Novermber 12th 2010 BY 5:00pm in ESB 3231C

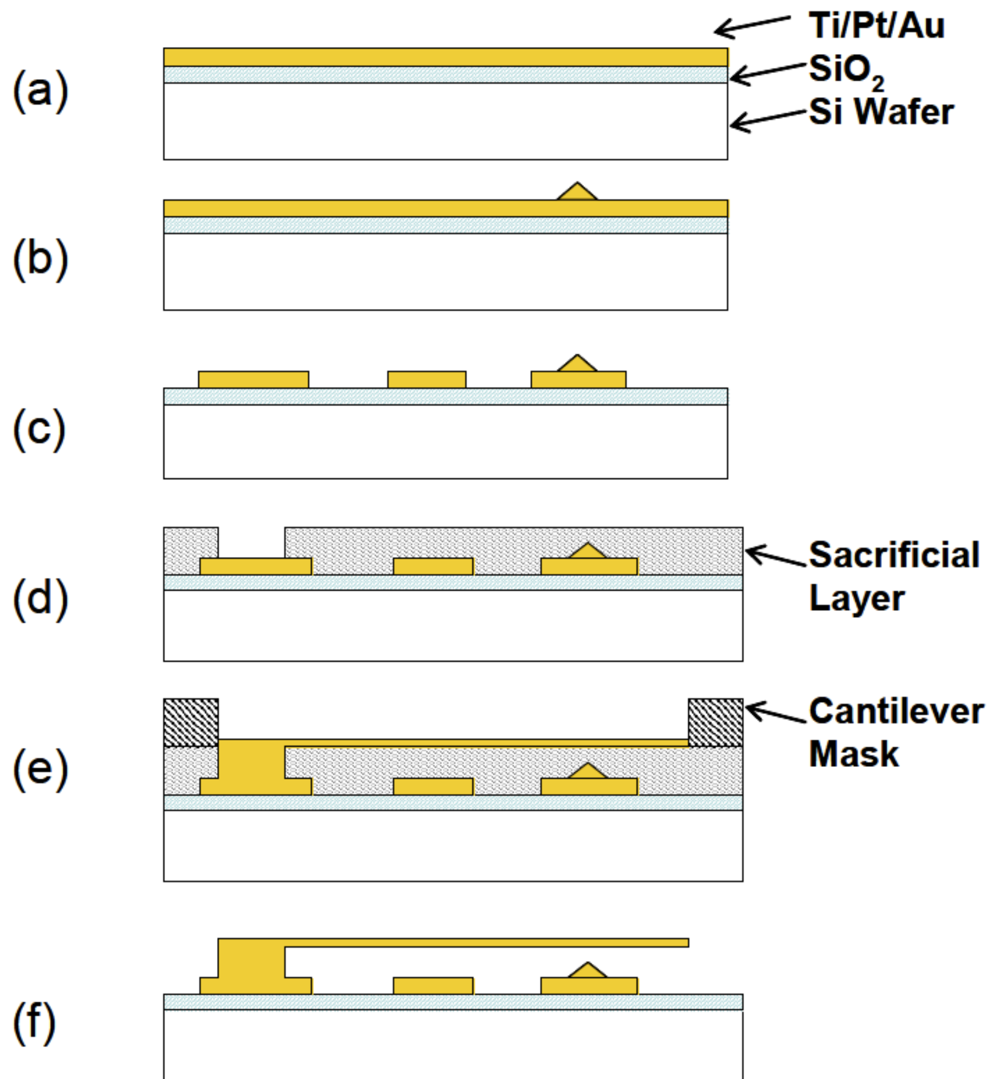
Problem #1: Tunneling Accelerometer Design Process

You are a young junior faculty member who has just hired your third graduate student, Perry Winkelmyer. You have developed an idea for using a surface-micromachined tunneling accelerometer. Remember, accelerometers are mechanical or electromechanical devices used for the measurement of acceleration or deceleration. Roughly, there are a combination of two transducers, one which measures the acceleration and converts it in terms of displacement and the other which converts the results into an electrical signal. Tunneling tips have been utilized to increase resolution and sensitivity over the miniaturization of accelerometers based upon piezoresistive, piezoelectric or capacitive transducers. Since electron tunneling can only be observed when the gap between the electrodes is near the order of 1 nm, the size constraint of a tunneling accelerometer must be of the same order. By utilizing a feedback control circuit to maintain a constant tunneling gap between tip and counter-electrode, the accelerometer is able to maintain minute displacement readings. The accelerometer has two major components, a single proof-mass component and a tunneling tip electrode.

Being a seasoned MEMS designer, you immediately notice several critical errors with Perry's process (things that won't work or won't produce the result that Perry shows in his cross sections). Please find the critical errors in this process flow and, where possible, suggest alternate approaches. Do not worry about the accumulation of errors, but rather treat each step assuming that the structure up to that step could be created.

Process steps:

1. Start with a Silicon Wafer. (a)
2. PECVD deposit 1 µm of SiO_2. (a)
3. E-bean evaporate 5 nm of titanium, 1 nm of platinum, and 200 nm of Gold. (a)
4. Grow tunneling tip on the metal layer through FIB lithography and ion milling. (b)
5. Perform photolithography using positive photoresist (not shown) and wet etch the electrode geometry using appropriate metal etchants. (c)
6. LPCVD deposit 1 µm of polysilicon as a sacrificial layer for gold cantilever (d)
7. Perform photolithography using positive photoresist (not shown), and wet etch the polysilicon using KOH to define the gold base for the cantilever. (d)
8. Deposit another layer of resist, and evaporate the Gold onto the sacrificial layer. (e)
9. Release the cantilever by etching the polysilicon with KOH. (f)



Problem #2:

In this design problem, we want to design and build an integrated microfluidic device with a polysilicon heater for PCR amplification of DNA, and then an injection channel for DNA separation and integrated electrodes for detection and identification.

Design schematics: polysilicon heater is denoted in orange, metal electrodes are denoted in black; channels and ports are in blue; oxide in the port areas is selectively etched to allow access to the channels.

Channel composition: The channel walls should be either oxide or nitride wherever possible. There cannot be polysilicon or metal directly in contact with the working

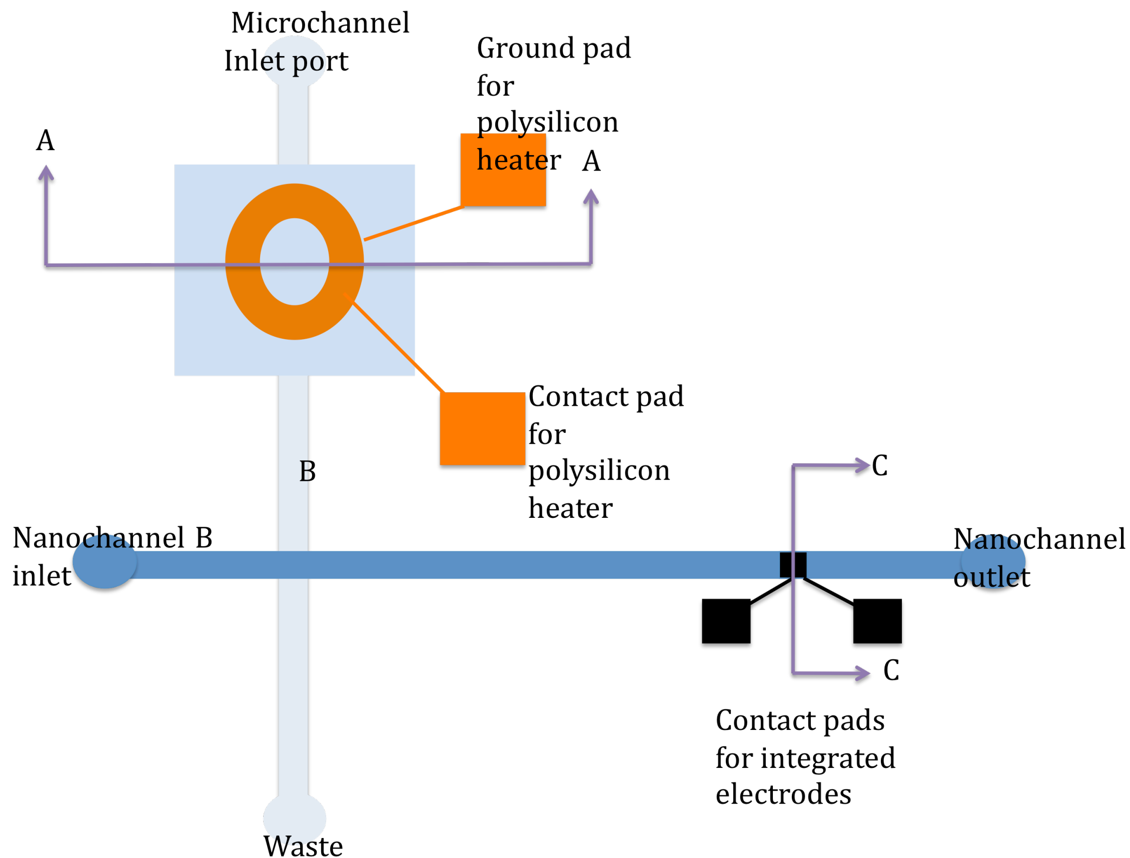
fluid. For the DNA amplification chamber, the polysilicon heater is on the bottom of the channel attached to a contact pad (Section A—A), but for detection in the nanochannel, the metal is both above and below the nanochannel, and also address by the contact pad (black). The order of the layers is not specified up front; you can pick any order that is feasible.

Dimensions of channel: 7 mm long, 10 μm wide, 100 nm high. HINT: think carefully about what starting substrate you are going to use, and whether you will choose a bulk or surface micromachining process.

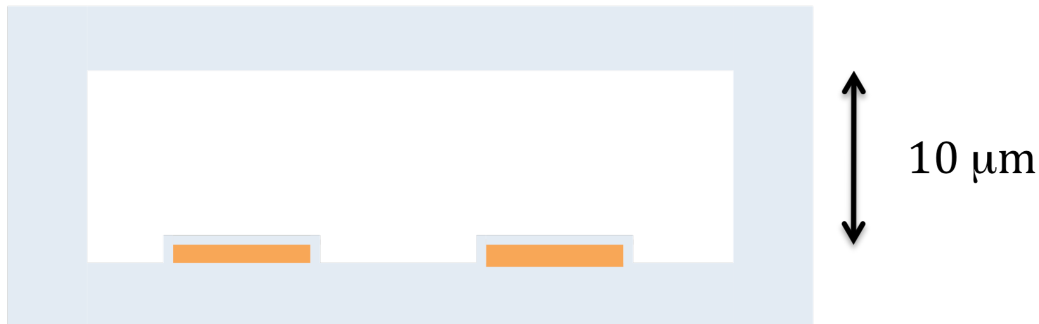
Metal layer: at least 50 nm thick.

Polysilicon: Doped (to act as heater) and about 1 micron thick.

Design Schematic



A----A cross section



C----C cross section

(a) It is useful to identify the challenges of the process flow (those points where we must be particularly careful to obey the laws of physics) early on. Examples could include thermal compatibility, chemical compatibility, and the ability to pattern the device geometry. Identify what you see as the major challenges for this process (a few words each). Pick three, and explain why they are an issue.

(b) Brainstorm three different ways of approaching the process, and explain them briefly. You don't have to have all of the details ironed out on these approaches.

(c) Choose one approach and flesh it out. You need to sketch the mask set with key dimensional relations and write out the steps of the process flow. Specify materials and the proposed deposition and etch methods, and be sure to include as steps in your process the required wafer cleans, application of photoresist, and stripping of photoresist. If a dimension on the mask affects the success of the process, make sure you specify it. Be sure to show cross-sectional and planar views of all key steps in the process. HINT: It may be easier for you to design the mask set needed in L-edit, and print those out. It is not required, but I have found it helps with the thinking process.