ME 141B: The MEMS Class Introduction to MEMS and MEMS Design

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Outline

- Class odds and ends
- Intro to MEMS
- The Challenge of MEMS Design
- Course Outline
- Microfabrication Overview

Handouts

- Syllabus/Schedule Handout
  - Lecturer: Prof. Sumita Pennathur
  - Text: Cambell Fabrication Mehods
  - Grading policy

- L-Edit Basics
  - First Assignment, due 10/7
  - E-mail .tbd file, turn in print-out

Handouts

- Lecture Notes
  - Handed out at the beginning of class
  - Will be posted online

- Safety Training Class 10/5
  - 10 people first half of class
  - 10 people second half of class
  - MANDATORY attendance

Course Overview

- First week – Overview
- Weeks 2 – 7 : Processing and Modeling
- Weeks 8 – 10: Case Studies

- Labs:
  - First 5 weeks – training
  - Next 5 weeks – you are on your own

Course conduct and ethics

- We encourage teamwork for lab reports, homeworks
  - ➢ L-edit, mask design, HW#1 and lab reports must be written up individually
- Cooperation is essential in final lab report
- No cooperation is allowed on the take-home midterm
- Any breaches will be dealt severely, with no warnings

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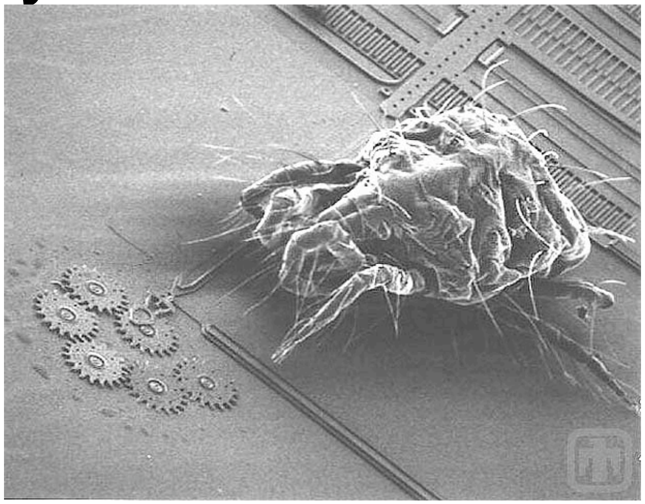
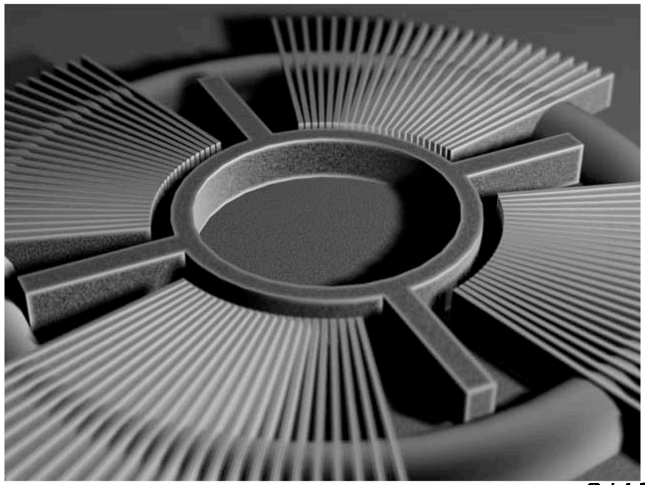
What are MEMS?

- Micro-Electro-Mechanical Systems
- Microsystems
- Microfabrication
- Microtechnology
- Nanotechnology
- Etc…





What are MEMS?

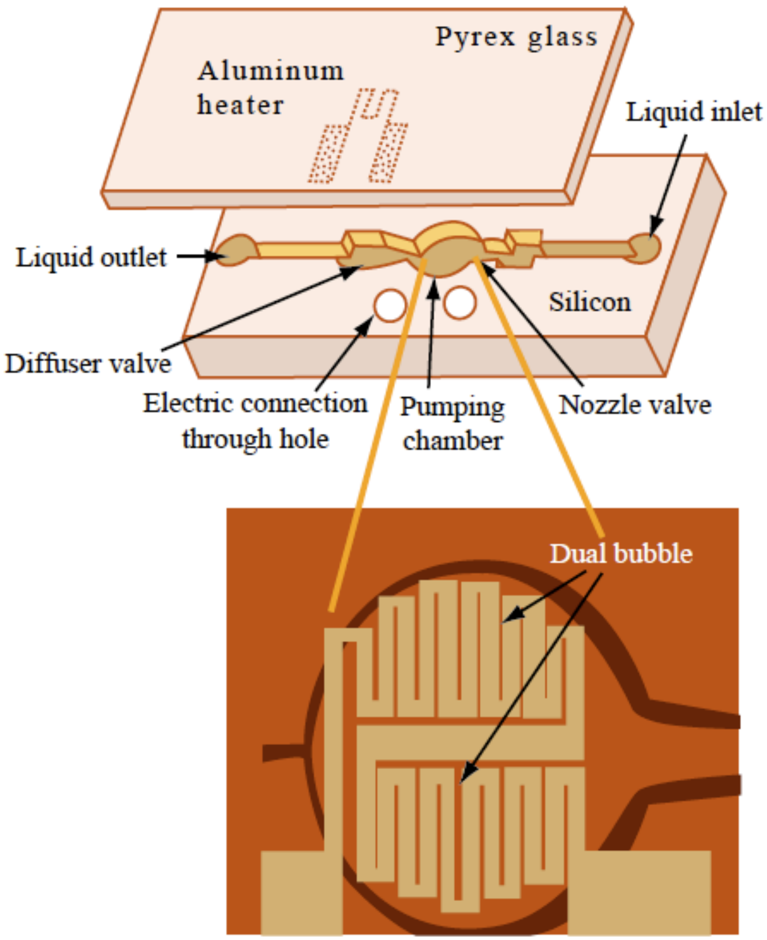
- Microfabrication is a manufacturing technology
  - A way to make stuff
  - Adapted from semiconductor industry
    - With changes
  - Therefore, MANY standard design principles hold
- But, has unique elements
  - New Materials : SU-8, PDMS
  - New ways to shape them: DRIE
  - New material propertes
    - Bulk vs. thin film
  - Different physics Regimes
    - Si at small scales

What are MEMS?

- Definitions vary
  - ➢ Usually made via semiconductor batch fabrications
  - ➢ Usually small
    - Some important dimension is <1 mm
  - ➢ Ideally, useful
  - ➢ Used to be actual electro-mechanical systems
    - ➢ Sensors: Something moves and is sensed electrically
    - ➢ Actuators: An electrical signal moves something

What are MEMS?

- Now, many “MEMS” have no “E” or “M”
  - ➢ Static microfluidic structures
  - ➢ But often are multi-domain
  - ➢ Electro- other domain is very popular
    - E.g., electro-thermal-fluidic-actuation
    - Microbubble pumps



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MEMS: History

- Some starting points:
  - ➢1961 first silicon pressure sensor (Kulite)
    - Diffused Si piezoresistors mounted onto package to form diaphragm
  - ➢Mid 60's: Westinghouse Resonant Gate Transistor
  - ➢Mid 70's Stanford Gas Chromatograph (1975)
    - Way ahead of its time

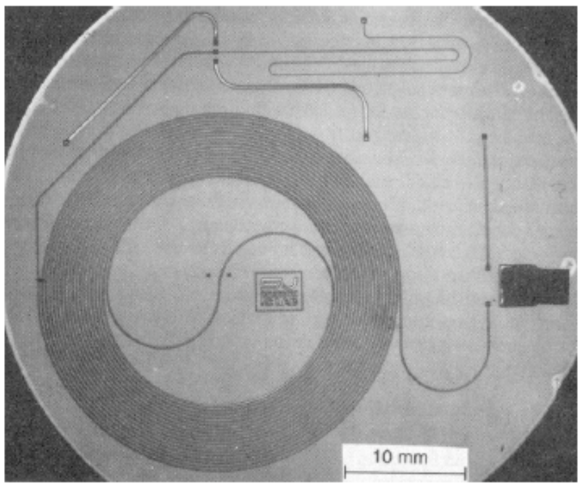
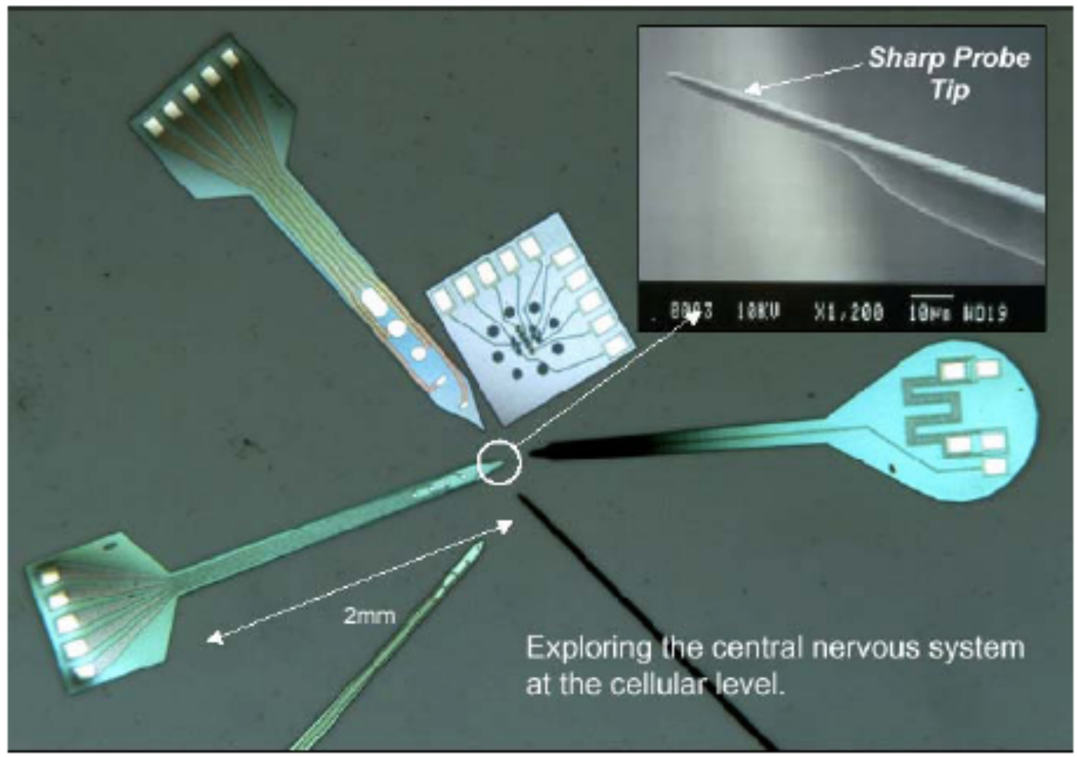


Figure 3 on page 1882 in: Terry, S. C., J. H. Jerman, and J. B. Angell. "A Gas Chromatographic Air Analyzer Fabricated on a Silicon Wafer." IEEE Transactions on Electron Devices 26, no. 12 (1979): 1880-1886. © 1979 IEEE.

MEMS: History

- 70’s to today: Ken Wise (Michigan) neural probes
- inkjet printers



Courtesy of Kensall D. Wise. Used with permission.

MEMS : History

- MEMS blossomed in the 80s
- 1982 Kurt Petersen "Silicon as a mechanical matieral"
- Mid 80's BSAC folks (Howe, Muller, etc..) polysilicon surface micromachining

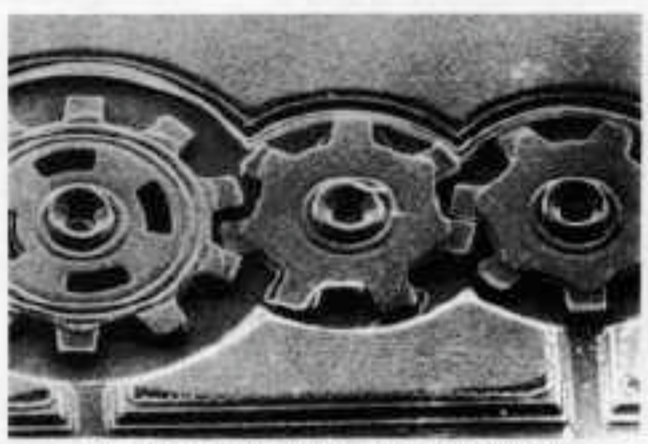
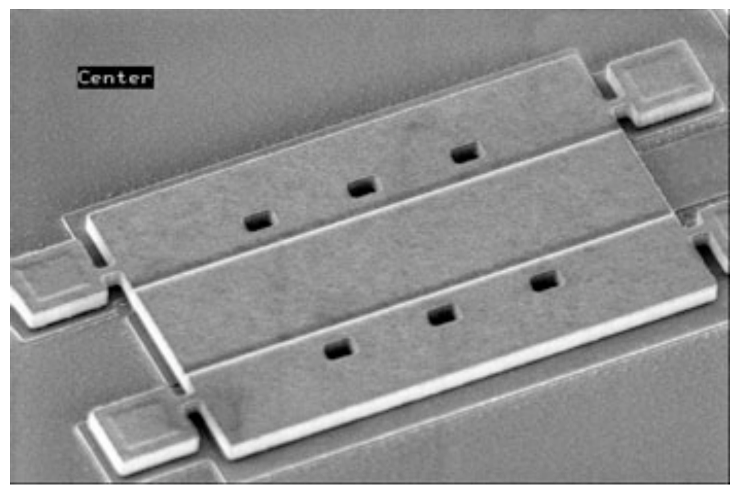
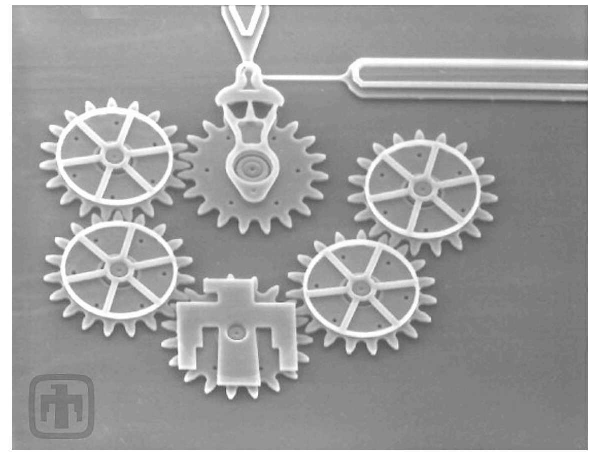


Fig. 4. The gear-train after being released and moved.



MEMS: History

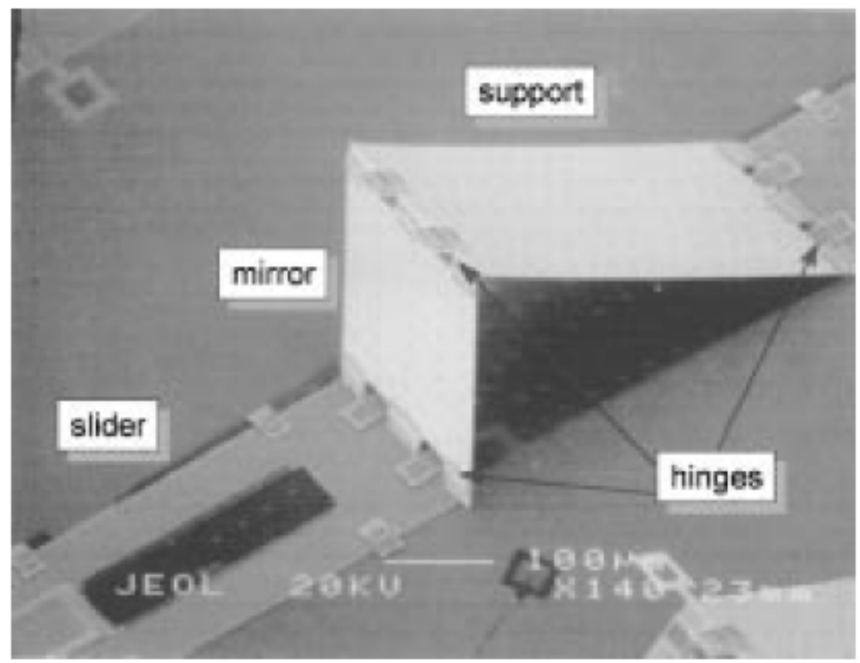
- Electrostatic Micromotors
  - ➢Introduced in 1988-1990
  - ➢MIT and Berkeley
- Microchip capillary electrophoresis and lab-on-a-chip
  - ➢Introduced ~1990-1994
  - ➢A. Manz, J. Harrison, etc..



MEMS: Current Topics

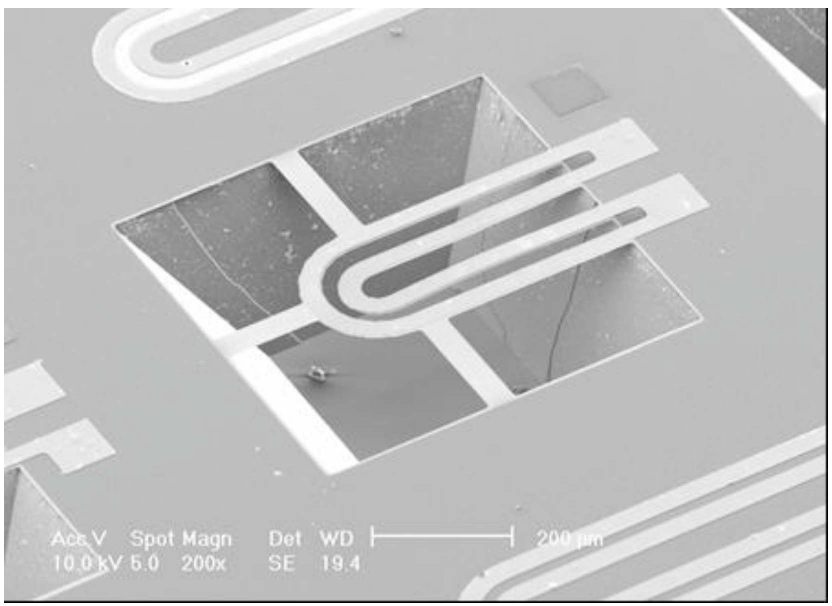
- Optical MEMS
  - Switching of optical signals
  - Big boom in the late 90's
  - Big bust in the early 00's

Lucent micromirror

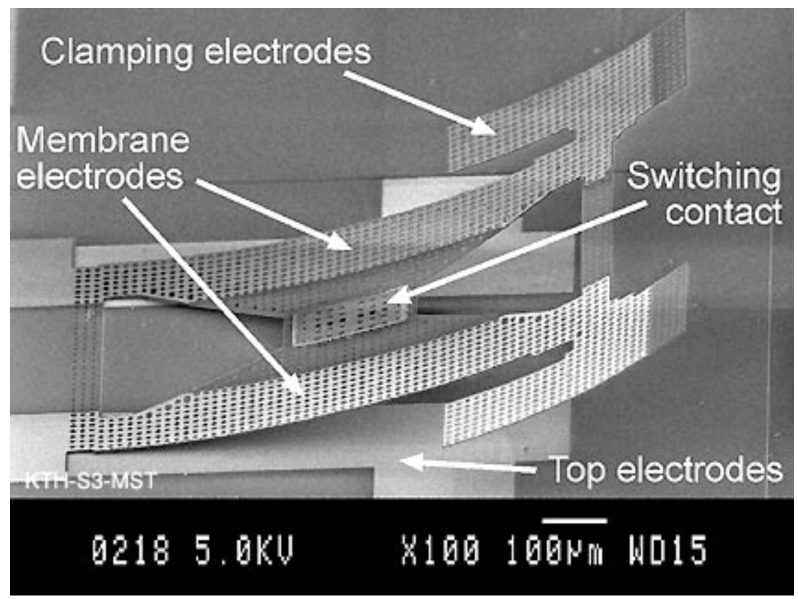


MEMS: RF MEMS

- Smaller, cheaper, better way to manipulate RF signals
- Reliability is issue, but getting there



Tunable inductor



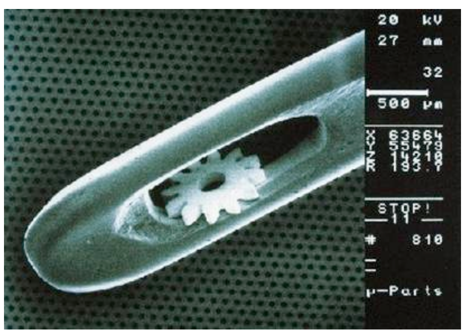
RF Switch

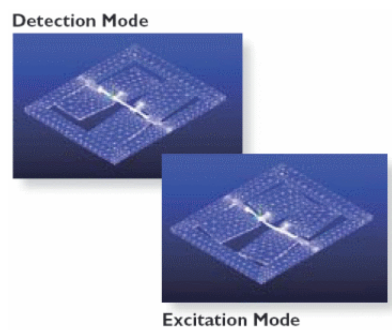
MEMS: BioMEMS

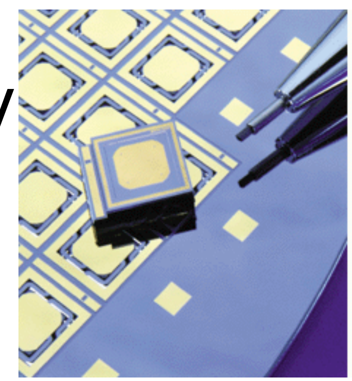
- Shows promise for diagnostics
- Next Era of Quantitative Biology
- No commercial winners yet

MEMS: Commercial

- This isn’t just academic curiousity
- There are products you can actually BUY
  - ➢Pressure sensors in your car & in your body
  - ➢Accelerometers EVERYWHERE
  - ➢Gyroscopes
  - ➢Ink-jet print heads
  - ➢Texas Instruments’ micro-mirror array







MEMS: Commercial

- The major successes have been pressure and inertial sensors
  - Most mature: 40+ ears
  - Huge initial market: automotive
  - Recent access to huger commercial market
  - Easy access to physcial signal
  - Smaller than alternatives
  - Cheaper than alternatives
    - ➢ In medical Market, that means disposable
  - Can be integrated with electronics
  - Moderately precise & accurate

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MEMS Design

- For our purposes, design means
  - ➢Create a device or system
  - ➢With quantitative performance parameters (e.g., sensitivity)
  - ➢Subject to constraints
    - Size, price, materials, physics
    - Some clearly defined…some not
  - ➢This is hard no matter what the device is

MEMS Design

- MEMS design is hard because
  - The manufacturing technology is actually quite imprecise
    - 10% tolerance on in-plane dimensions is typical
    - Out-of-plane tolerances may be much better….or much worse
    - Fabrication success is NOT a given AND is tied to the design
    - The material properties are unknown or poorly known
    - The physics are often “different”
      - Not the traditional size scales
    - The system must be partitioned
      - Which parts can you integrate on-chip?
    - Packaging is non-trivial
      - NOT like ICs

All these questions should be answered EARLY ON

Some solutions to this challenge

- Approach #1
  - Make something easy or not useful, etc..
- Approach #2
  - Do incorrect back-of-the-envelope design and then proceed
- Approach #3 (grad student favorite)
  - Create a large range of structures → One of them will work, *hopefully*
- Approach #4 (the MEMS class way)
  - Predictive design of all you know to enable chance of first round success
  - Determine necessary modeling strategies for a given problem
  - Be aware of what you don't know, can't control, and what your assumptions are

MEMS Design

- Different levels of design
  - Analytical design
    - Abstracted physics
    - ODEs, Scaling, Lumped-element models
  - Numerical Design
    - Intermediate approach between physical and analytical design
  - Physical level:
    - 3D simulation of fundamental physics
    - PDEs, finite-element modeling, etc…
- Tradeoff between accuracy and effort/time
- Always limited by fundamental knowledge of properties or specifications

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Course Goal

- Course goal: Learn how to design/fabricate any microfabricated device/system
- Learn how to
  - Understand the design process
  - Partition the system
  - Determine and model relevant physics
  - Evaluate different designs & fabrication techniques
  - Understand the linkage between fabrication and design

Course Outline

- First up: fabrication proceses
  - Lithography
  - Etching
  - CVD
  - Evaporation, Sputtering
  - Moxidation
- MEMS Design
- MEMS case studies

Course outline

- MEMS fabrication is intimately coupled with design
  - ➢Not true of many other worlds
  - ➢Example: diaphragm pressure sensor
    - Would like to use Si because of piezoresistors
    - Material choice sets fabrication technology: KOH
    - Fabrication technology determines shapes and physical limits: diaphragm thickness
    - This in turn affects performance

      Deflection ~ (thickness)^-3

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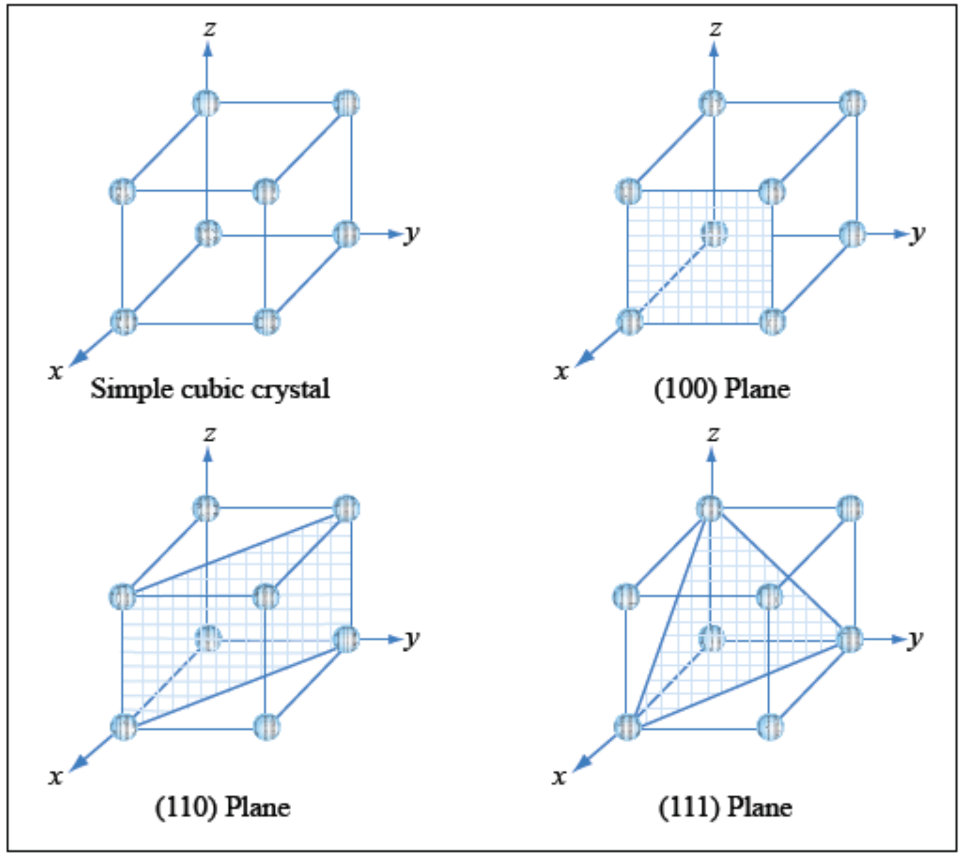
Microfabrication Outline

- Substrates
- Lithography and patterning
- Doping
- Thin Films

Substrates: Silicon

- Silicon is a diamond-structure cubic crystal
- Comes with different amount of either n-type or p-type doping

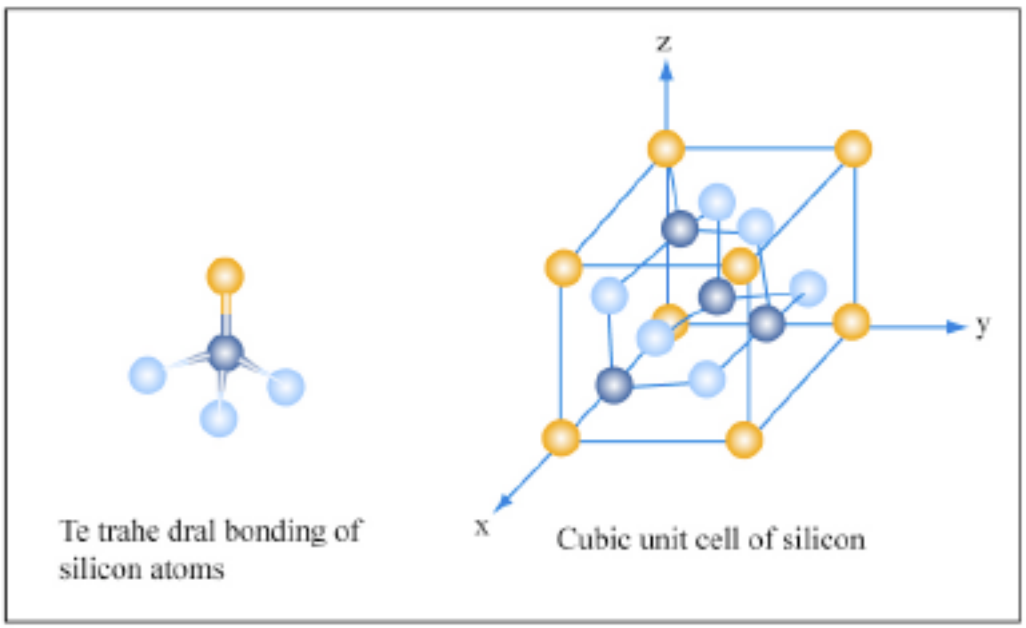


Silicon: Notation

- A direction in crystal coordinates in denoted by square brackets, e.g. [100]
- The set of symmetrically equivalent directions is written with braces, e.g. <100>
- The plane perpendicular to a direction is denoted with parentheses, e.g. (100)
- The set of symmetrically equivalent planes is written with curly brackets, e.g. {100}

Silicon: Diamond Structure

- The diamond structure is two face-centered cubic lattices shifted by ¼ of the body diagonal. There are four silicon atoms per cubic unit cell.



Wafer Orientation

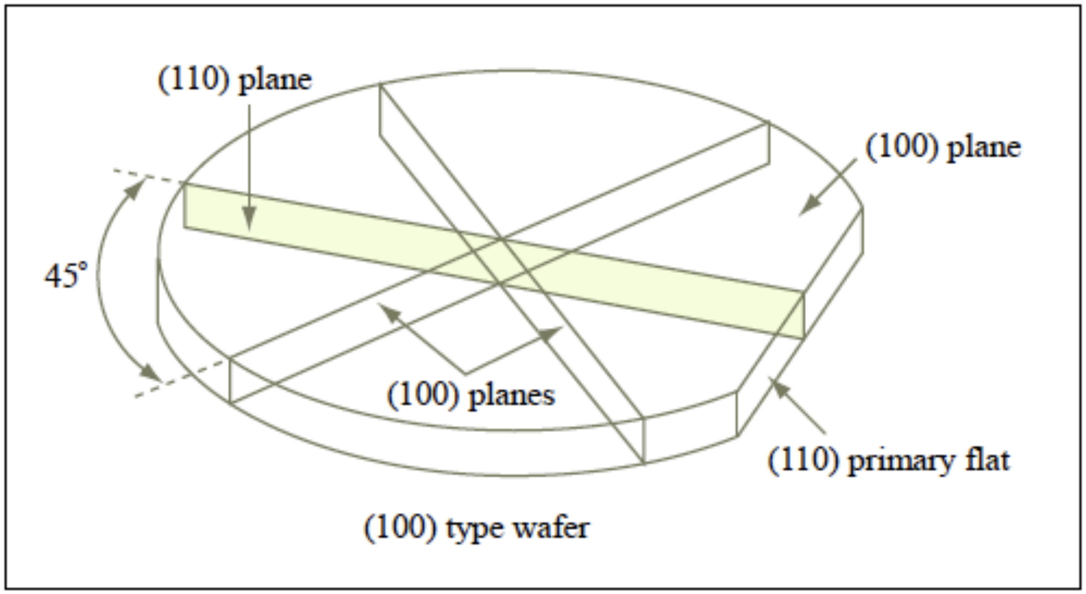
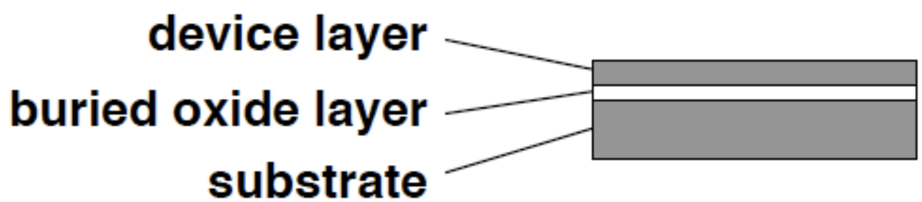


Image by MIT OpenCourseWare.
Adapted from: Maluf, Nadim. *An Introduction to Microelectromechanical Systems Engineering*. Boston, MA: Artech House, 2000. ISBN: 9780890065815.

Picture from N. Maluf, An Introduction to Microelectromechanical Systems Engineering

SOI

- Silicon wafers with embedded layers, such as silicon-on-insulator (SOI) wafers



- Initial purpose: build IC's on device layer, and buried oxide minimized stray capacitance to substrate
- Common MEMS purpose: bulk micromachining top layer into moveable structures with well-controlled thickness

Other substrates

- Glass (cheap, high impurity content)
  - Inexpensive base for soft lithography
  - Transparent for optical access
  - Can be very strongly attached to silicon wafers via anodic bonding
- Quartz/Fused silica
- Compound semiconductors
  - Optical applications
- Plastics
- PDMS
- Titanium
- Sapphire
  - Strong, wear resistant, transparent, insulating substrate
  - Compatible with CMOS (so transparent CMOS MEMS)
  - Expensive, hard to etch

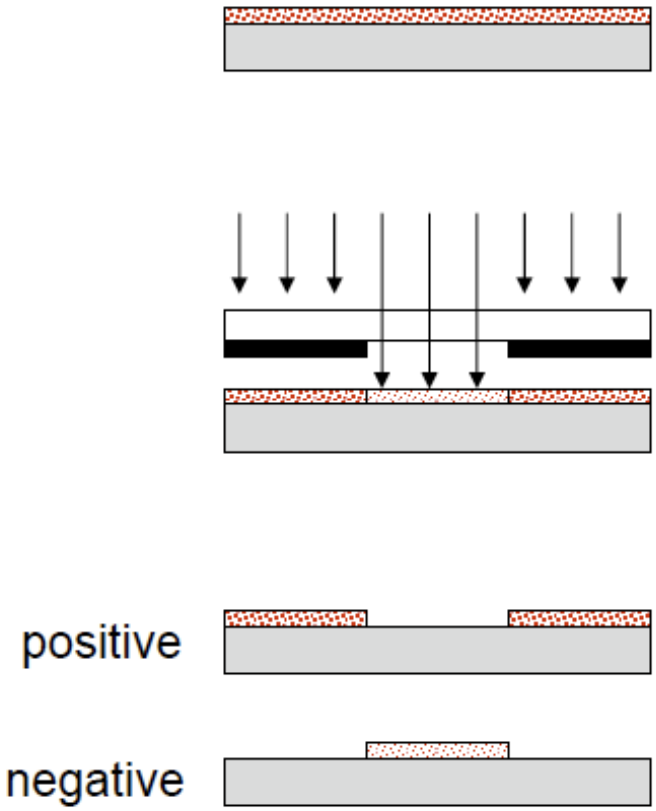
Substrate Summary

Substrate	Front end compatible	Back end compatible	Everything else compatible
Silicon	yes +	yes	yes, but only use if needed
Silicon on insulator (SOI)	yes +	yes	yes, but only use if needed
Quartz	yes	yes	yes, but only use if needed
Glass (pyrex)	no	yes, sometimes	yes +
Compound semiconductor	no	yes	yes, but only use if needed
Sapphire	yes, but only use if needed	yes, but only use if needed	yes, but only use if needed

Microfabrication Outline

- Substrates
- Lithography and patterning
- Doping
- Thin Films

Optical Lithography



Spin-cast a photosensitive resist layer; bake out solvent

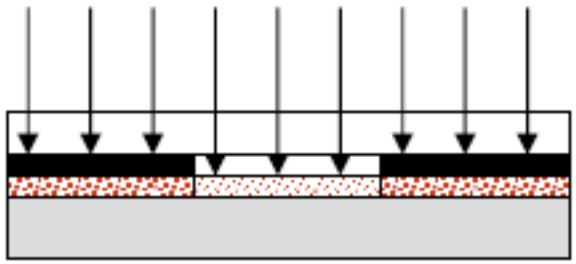
Collimated UV exposure through a mask; resist either cross-links or becomes soluble

Develop by dissolving the exposed/unexposed (positive/negative) resist; can now transfer pattern to substrate

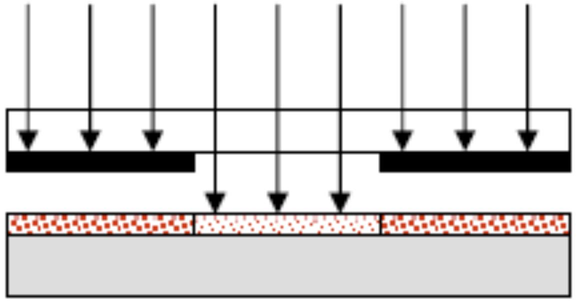
Alignment fiducials permit alignment of subsequent masks.

Methods of optical lithography I

- Contact
  - ➢ Mask touches wafer
  - ➢ Inexpensive
  - ➢ Contact degrades mask
  - ➢ No die size limit
  - ➢ Resolution: down to 1 micron nervously; down to several microns comfortably



- Proximity
  - ➢ Mask of order 10 microns from wafer
  - ➢ Inexpensive
  - ➢ Less mask damage
  - ➢ Diffraction means lower resolution
  - ➢ No die size limit
  - ➢ Resolution: down to several microns nervously, somewhat larger comfortably



Projection Lithography

- Projection lithography, especially when combined with an optical imaging system that reduces the image size, is used for high-resolution patterning (submicron to very submicron)
- Larger mask features, no contact with mask
- Wafer steppers expose one die at a time, assuring good focus and registration
- Something to consider: if your device needs a fine features, a stepper may be required. But steppers have limits on dies size of about 1 cm.

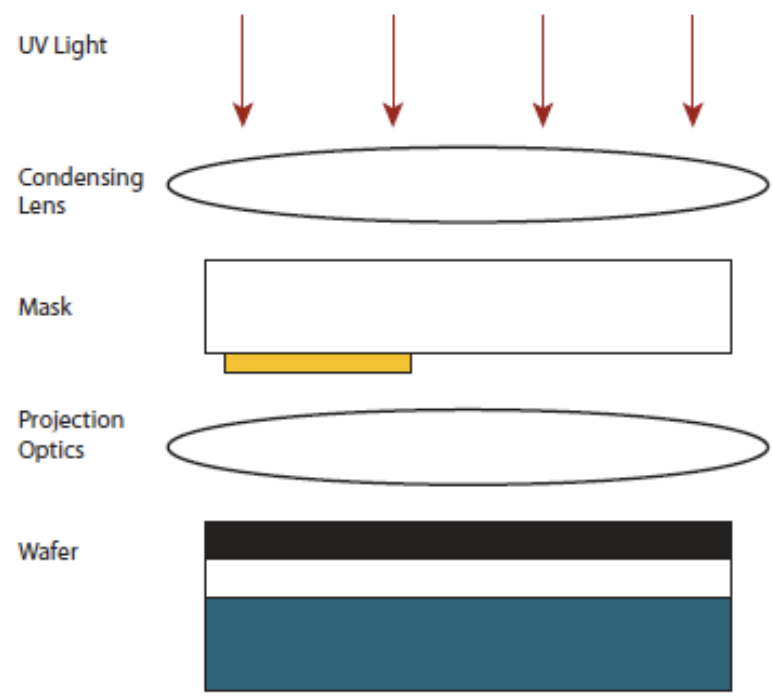


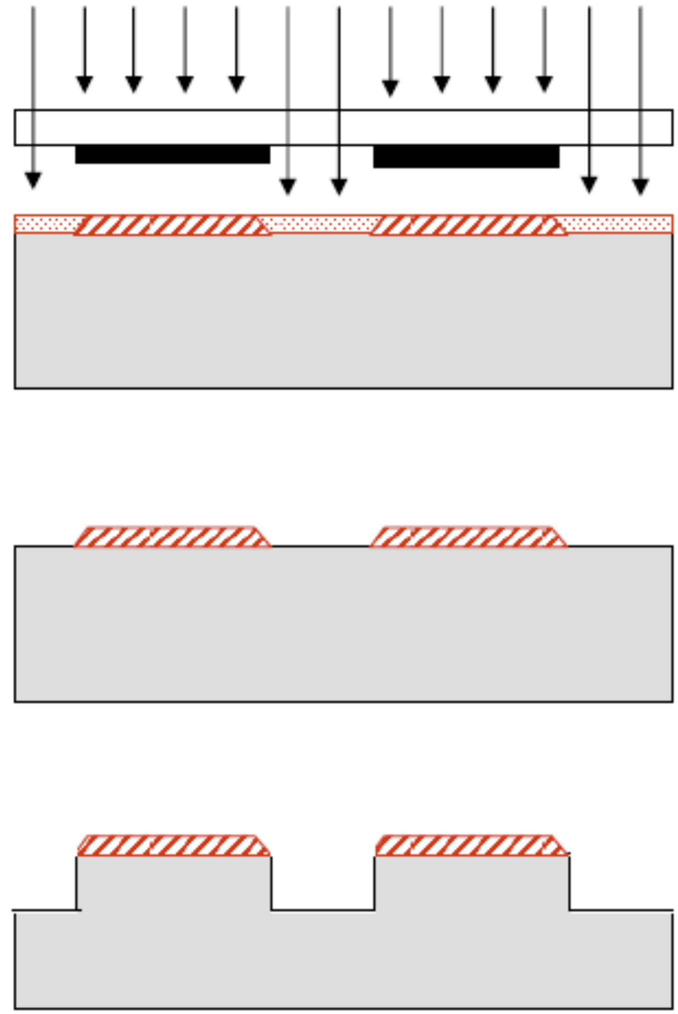
Image by MIT OpenCourseWare.
Adapted from Figure 3.15 in: Senturia, Stephen D. *Microsystem Design*. Boston, MA: Kluwer Academic Publishers, 2001, p. 53.
ISBN: 9780792372462.

Mask Making

- Highest quality – chromium on fused quartz written with an electron beam exposing an electron-beam resist (PMMA)
  - Also very high quality: laser-writing
- Photographic emulsion on fused quartz exposed with UV light flashes through a programmable aperture
- Patterns printed from an L-EDIT file on transparencies with a very high-resolution printer – low resolution, but cheap and fast

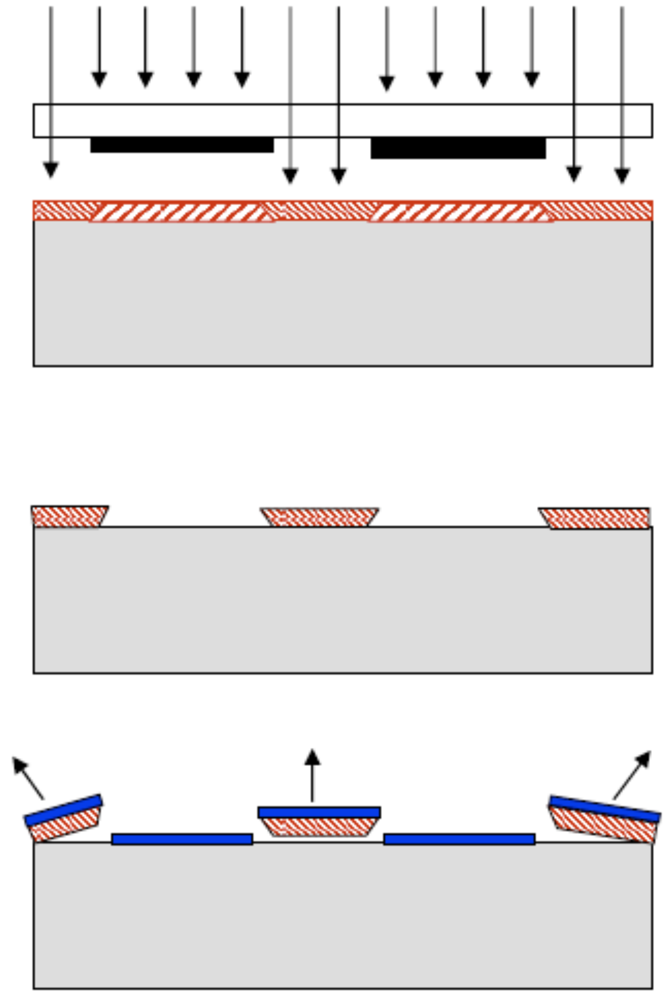
Positive thin resist

- Spin cast
- Thickness of order 1 micron
- Developer removes exposed resist
- Creates sloped profile at resist edge
- Some applications
  - Wet etching
  - Shallow Dry Etching
- Front end standard



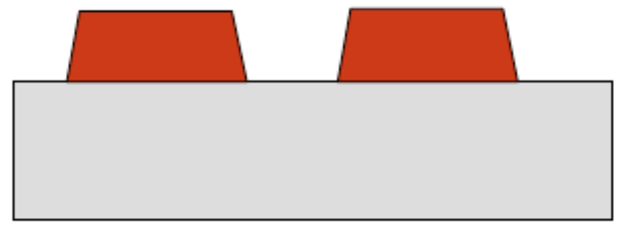
Negative/image reversal photoresists

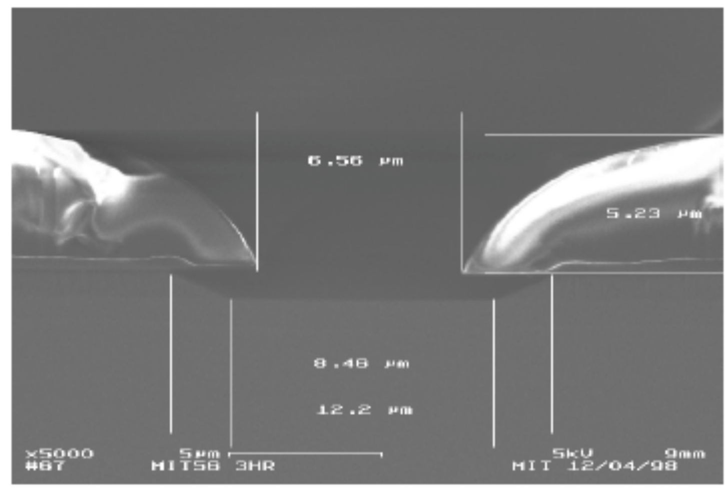
- Spin cast
- Thickness of order 1 micron
- Developer removes unexposed resist
- Creates a re-entrant profile
- Typical application: liftoff processes (in acetone), often seen in back end processing
- Rule of thumb: resist thickness should be 3x thickness of layer to be lifted off
- Not a standard front end material, but not inherently incompatible with it



Positive Thick Photoresist

- Spin cast
- Thicknesses of order 10 microns
- Sloped profiles
  - ➢ Slope somewhat controllable through process conditions
- Some planarizing capability
- Typical Applications:
  - ➢ Prolonged or low selectivity dry etch
  - ➢ Deep reactive ion etch
  - ➢ Masking any etch over topography
- Not a standard front end material, but not inherently incompatible with it





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Double-sided aligned lithography

- Goal: align features on the back of the wafer to features on the front
  - ➢Common requirement in bulk micromachining
  - ➢Not a standard IC capability
  - ➢Functionality more common as market grows
- What you need:
  - ➢Double side polished wafer
  - ➢Double sided alignment tool
    - IR alignment, registration to global fiducials in the tool, through holes, etc.

Special purpose lithographic techniques 1

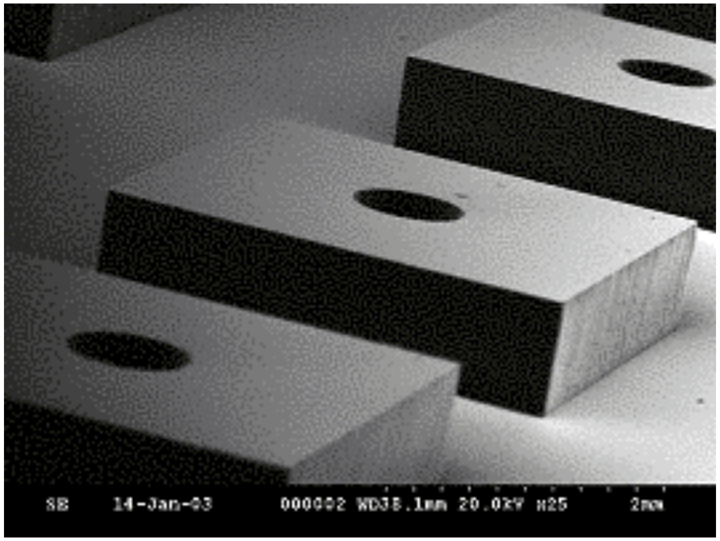
- X-Ray lithography
  - One application: making molds for LIGA (lithography, electroplating an molding)
  - Requires an x-ray source and x-ray mask
- Electron beam lithography
  - High resolution (tens of nanometers)
  - NEMS
  - A slow, serial process
- Lithographic techniques that are rarely seen in front end processing

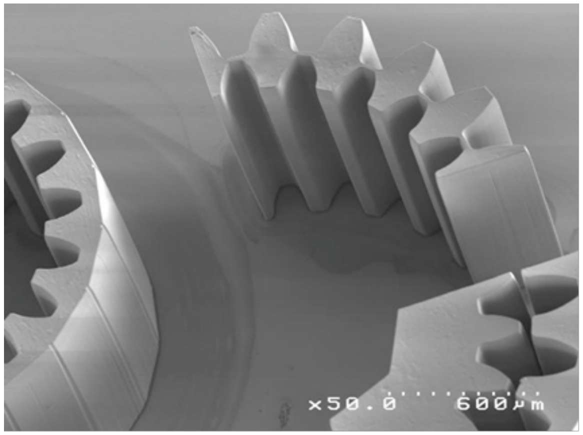
Special purpose lithographic techniques 2

- Shadow masking
  - Direct evaporation or sputtering through physical holes in a shadow mask (think stencils)
  - Back end/everything else process
  - “Last ditch” technique for patterning surfaces that cannot be coated with resist (large topography, fragile features)
- “Soft lithography”
  - Using PDMS as a physical mold to replicate structures
  - Advantages:
    - Patterning curved surfaces
    - Rapid, inexpensive fabrication

Very Thick Photoresists

- SU-8 epoxy
  - Spin cast
  - Negative resist, optical exposure
  - Can planarize extreme topographies
  - Can be structural, not easily dissolved
- Poyimide
  - Spin cast
  - Can planarize topographies
  - Humidity sensitive





Details that matter for lithographic processing

- Existing topography: if your existing feature heights are comparable to or greater than the thickness of the resist that you are putting down, you will not have good coverage
  - Incompletely covered sidewalls, holds full of resist, resist that never enters a hole at all
  - Solutions: eliminate the topography, thicker resist, alternate coating technology (spray on, electrophoretic resist?), use of a previously patterned hard mask instead of a resist mask
- Patterned resist does not have a square profile – can affect the topography of whatever you pattern with the resist
- Resist adhesion
  - If the surface of the wafer is hydrophilic (like SiO_2), the resist might peel during subsequent wet processing steps.
  - Surface preparation is key (e.g. dehydration bake and HMDS coating to render surface hydrophobic)

Cleaning!

- When we say (for example) that positive thin resist is compatible with front end processing, we do not mean that you can have resist on your wafer during most of the front-end process!
- Must remove resist and clean wafer thoroughly before any high temperature processes
- Always include cleaning in process flows, starting at the crayon engineering level
- Resist removal techniques
  - O2 plasma ash
  - Chemical removal of organics: piranha clean or nanostrip
  - Solvents (acetone)

More cleaning!

Additional cleans typically needed at specified points in the flow

Example: RCA clean before very high temperature processing (as in furnace for front end processing)

- **Step 1: Organic clean, 5:1:1 H_2O:H_2O_2:NH_4OH at 75 - 80C**
- **Step 2: Thin oxide removal, 50:1 H_2O:HF**
- **Step 3: Metal/ionic contamination removal, 6:1:1 H_2O:H_2O_2: HCl at 75 – 80C**

Example: remove organics before moderately high temperature, fairly clean processing (upper part of back end processing)

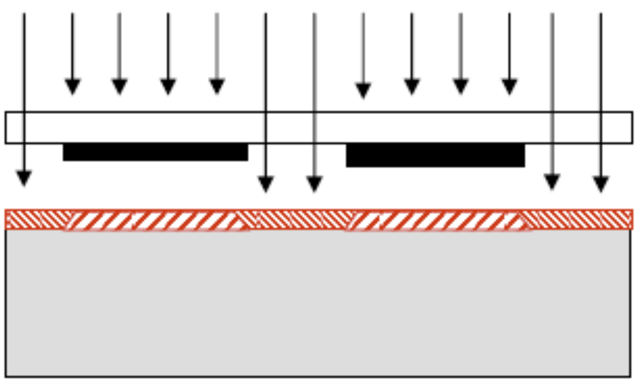
- **Piranha clean (3:1 H_2SO_4:H_20_2)**

Materials compatibility (what cleans your structures can tolerate) often determine what processes you can and can't use

If you wait until the last minute to put cleans into your process flow, you will likely be redesigning your device and process at the last minute

Another important detail: process bias

- The feature drawn on the mask is NOT the same size as the feature produced on the wafer
- Exposed area usually extends beyond clear area on mask
- Resist selection impacts process bias
  - Resist thickness
  - Resist Tone



Design Rules

- Alignment of one pattern to the next is critical to device fabrication
- Design rules are created to assure that fabrication tolerances do not destroy devices