



ME 141B: The MEMS Class

Introduction to MEMS and MEMS Design

Sumita Pennathur
UCSB





Outline



- Class odds and ends
- Intro to Your Device
- Process Flow for Your Device
- Microfabrication Outline



Suggested groups



Group 1	Group 2	Group 3	Group 4	Group 5
Simon Bill	Gina Adam	Dustin Chavez	Peter Herbert	Jared Frey
Charles Garcia	Hong Li	Tyler Hatlen	Steven Wehmeyer	Brian Hoffman
Group (6)	Group (7)	Group (8)	Group (9)	Group (10)
Jarred Hare	Ludovico Megalini	Louis VanBlarigan	Travis O'Donnell	Burga Kaytanli
Ashok Kodigala	Christian Gebbe	Miguel Zepeda- Rosales	Tyler Ray	Yuhui Ma



Safety Lecture!



- Thursday 12:30-2:15pm
- MANDATORY ATTENDANCE
- Lithography/cleaning training next week
 - Sign up on sheet
 - Groups 1&6, 2&7, 3&8, 4&9, 5&10 attend trainings together
 - Let me know ASAP if you need to change groups



Lab Report Information



- You will be learning how to make a specific device, and in the process you will have 3 lab reports due
- Lab Report I due 10/19
- Individual Lab Reports must be turned in, but do the work with your lab partner
- Must be professional quality work!
 - Remember, this is the bulk of your grade



Outline



- Class odds and ends
- Intro to Your Device
- Process Flow for Your Device
- Microfabrication Outline



Outline to your Device



1. Etching Channels

1. Solvent clean
2. Spin photoresist
3. Expose with opposite of the fluidic pattern
4. Develop photoresist
5. Deposit hard mask (Cr-Au)
6. Lift off
7. Wet etch (Buffered HF)
8. Metal etch

2. Depositing Electrodes

1. Solvent clean
2. Spin photoresist
3. Expose with metal pattern (aligned to fluidic features)
4. Develop photoresist
5. Descum
6. Evaporate Ti-Au
7. Lift off

3. Sealing the Channels

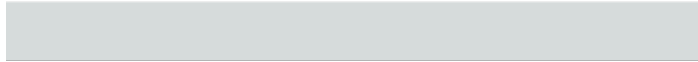
1. Prepare Flat PDMS (3-5mm Thick)
2. Punch holes (biopsy punch)
3. Clean
4. O₂ Plasma Treatment
5. Align and Bond
6. Run experiments



Etching Channels



Solvent Clean Sample



Spin Photoresist (PR)



Expose Sample



Orange: Exposed, Red: Unexposed



Develop PR



Evaporate Hard Mask (Cr-Au)



Lift Off

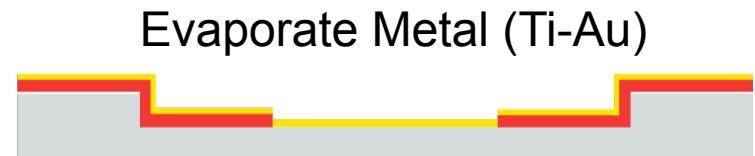
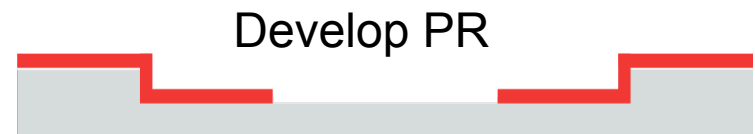
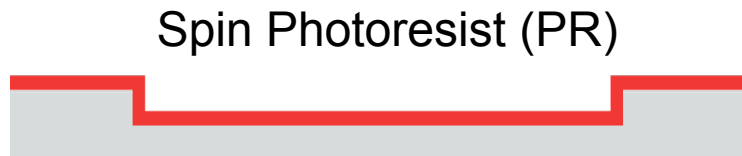
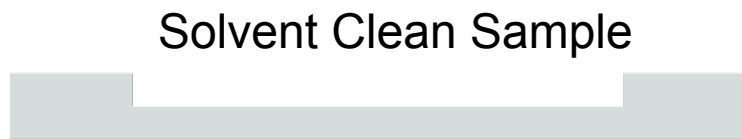


Etch Channel
Then Remove Metal





Depositing Electrodes

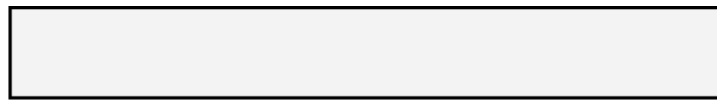




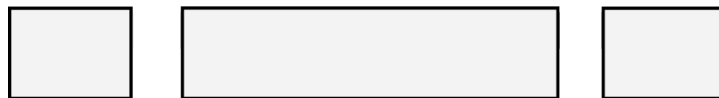
Sealing the Channels



Prepare Flat PDMS

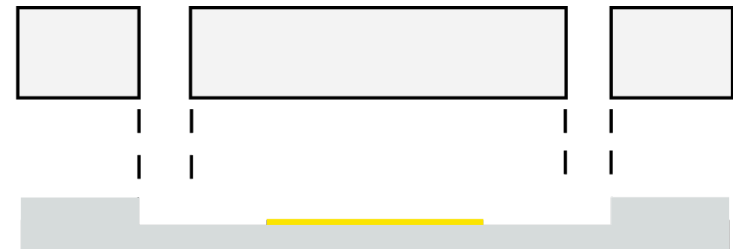


Biopsy Punch Access Holes

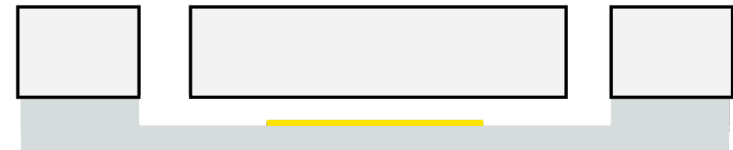


O₂ Plasma Surface Treatment

Align



Bond



Fill with Fluid



Perform Experiments



Process odds and ends



- Mask 2 (electrodes) will be given to you
- Mask 1 you must design yourself and print out on a transparency
- Substrates will be provided to you. Be wise with them!
- Next Week: Cleaning substrates, Lithography, inspection
- If you finish channel by Week 6, you may design and fabricate your own microfluidic/nanofluidic device
- Otherwise, focus on creating perfect micro/nano device
- Weeks 8-10: Characterization and testing of devices. You **MUST** have a working device by then!



Microfabrication Outline



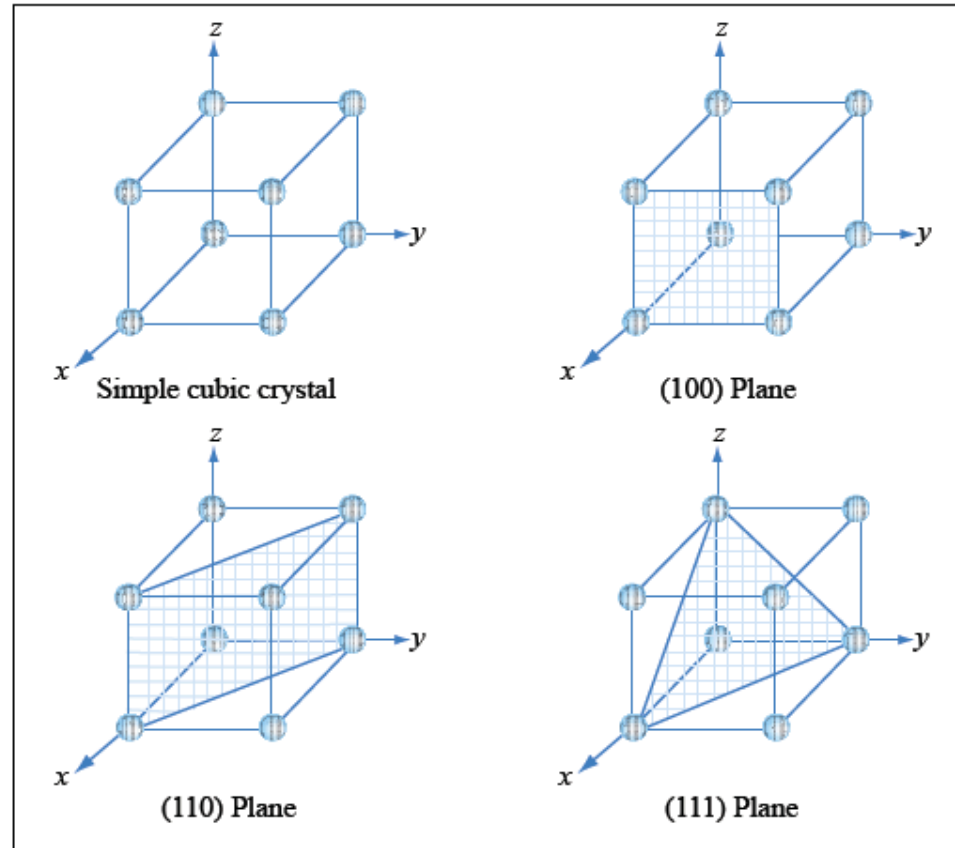
- Substrates – Si, SOI, Fused quartz, etc..
- Lithography and patterning
- Doping
- Thin Films
- Etching
- Wafer Bonding
- Surface Micromachining
- Process Integration



Substrates: Silicon



- Silicon is a diamond-structure cubic crystal
- Comes with different amount of either n-type or p-type doping

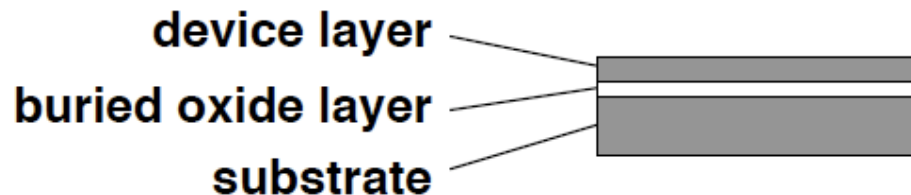




SOI



- Silicon wafers with embedded layers, such as silicon-on-insulator (SOI) wafers
- Initial purpose: build IC's on device layer, and buried oxide minimized stray capacitance to substrate
- Common MEMS purpose: bulk micromachining top layer into moveable structures with well-controlled thickness





Other substrates



- Glass (cheap, high impurity content)
 - Inexpensive base for soft lithography
 - Transparent for optical access
 - Can be very strongly attached to silicon wafers via anodic bonding
- Quartz/Fused silica
- Compound semiconductors
 - Optical applications
- Plastics
- PDMS
- Titanium
- Sapphire
 - Strong, wear resistant, transparent, insulating substrate
 - Compatible with CMOS (so transparent CMOS MEMS)
 - Expensive, hard to etch



Substrate Summary



Substrate	Front end compatible	Back end compatible	Everything else compatible
Silicon	yes +	yes	yes, but only use if needed
Silicon on insulator (SOI)	yes +	yes	yes, but only use if needed
Quartz	yes	yes	yes, but only use if needed
Glass (pyrex)	no	yes, sometimes	yes +
Compound semiconductor	no	yes	yes, but only use if needed
Sapphire	yes, but only use if needed	yes, but only use if needed	yes, but only use if needed



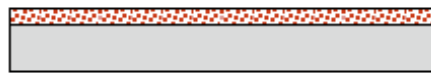
Microfabrication Outline



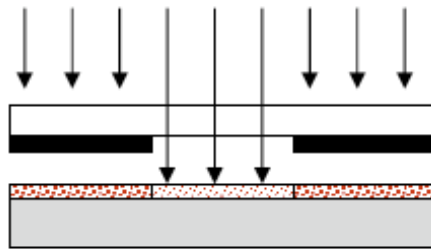
- Substrates – Si, SOI, Fused quartz, etc..
- Lithography and patterning
- Doping
- Thin Films
- Etching
- Wafer Bonding
- Surface Micromachining
- Process Integration



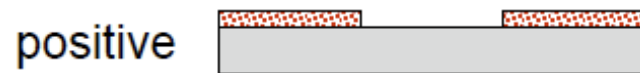
Optical Lithography



Spin-cast a photosensitive resist layer; bake out solvent



Collimated UV exposure through a mask; resist either cross-links or becomes soluble



Develop by dissolving the exposed/unexposed (positive/negative) resist; can now transfer pattern to substrate



Alignment fiducials permit alignment of subsequent masks.

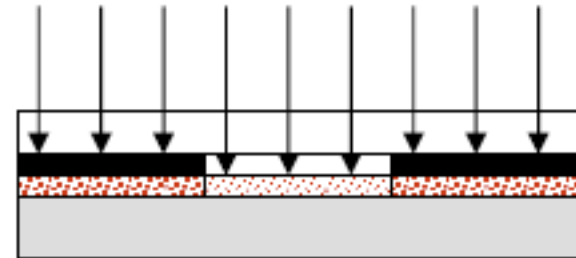


Methods of optical lithography I



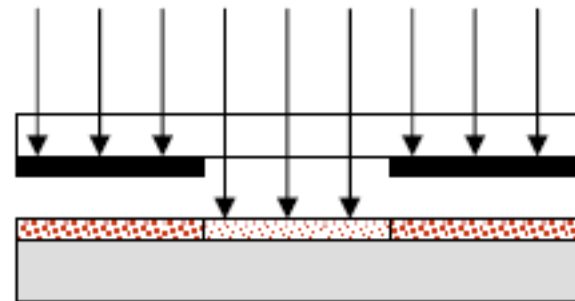
- Contact

- Mask touches wafer
- Inexpensive
- Contact degrades mask
- No die size limit
- Resolution: down to 1 micron nervously; down to several microns comfortably



- Proximity

- Mask of order 10 microns from wafer
- Inexpensive
- Less mask damage
- Diffraction means lower resolution
- No die size limit
- Resolution: down to several microns nervously, somewhat larger comfortably





Projection Lithography



- Projection lithography, especially when combined with an optical imaging system that reduces the image size, is used for high-resolution patterning (submicron to very submicron)
- Larger mask features, no contact with mask
- Wafer steppers expose one die at a time, assuring good focus and registration
- Something to consider: if your device needs a fine features, a stepper may be required. But steppers have limits on dies size of about 1 cm.

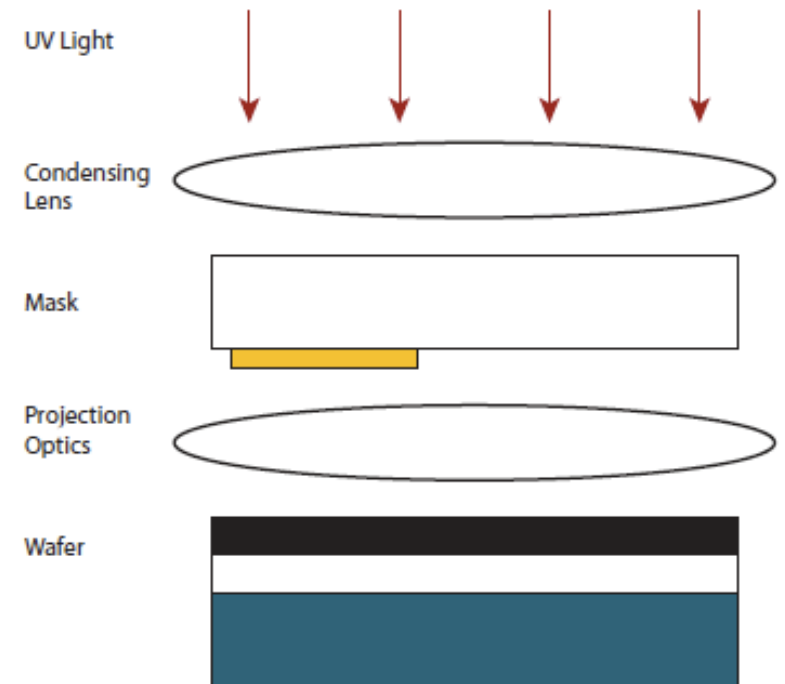


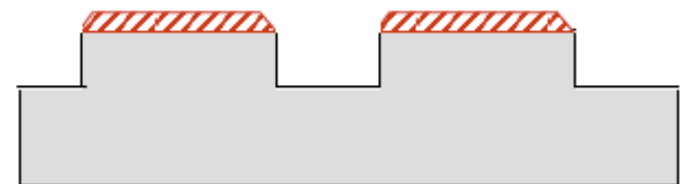
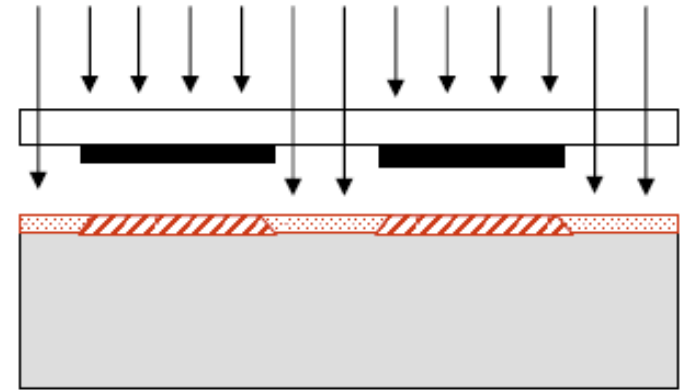
Image by MIT OpenCourseWare.
Adapted from Figure 3.15 in: Senturia, Stephen D.
Microsystem Design. Boston, MA: Kluwer
Academic Publishers, 2001, p. 53.
ISBN: 9780792372462.



Positive thin resist



- Spin cast
- Thickness of order 1 micron
- Developer removes exposed resist
- Creates sloped profile at resist edge
- Some applications
 - Wet etching
 - Shallow Dry Etching
- Front end standard

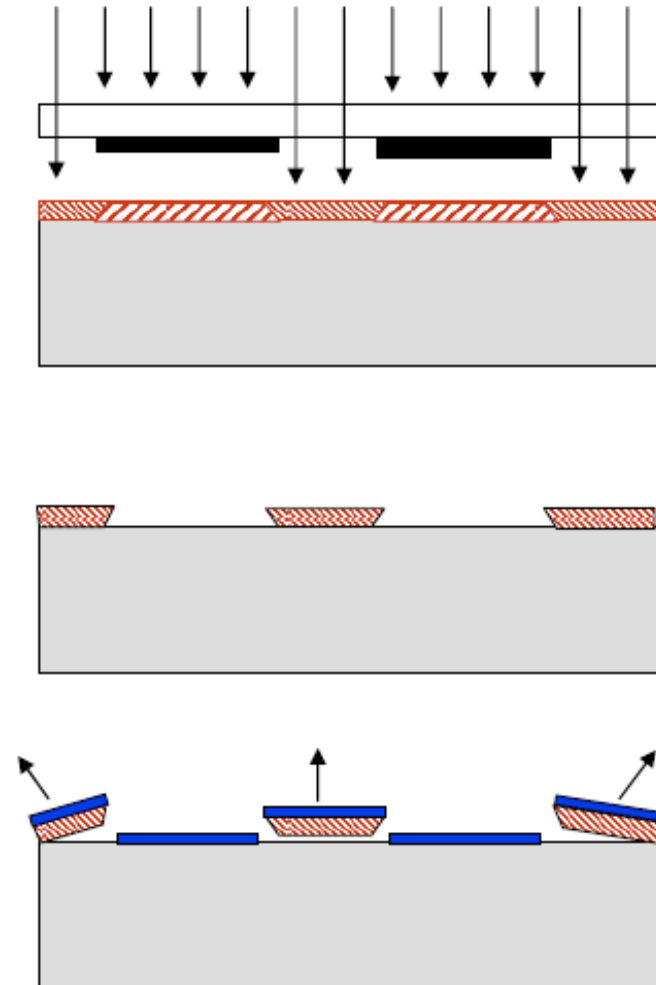




Negative/image reversal photoresists



- Spin cast
- Thickness of order 1 micron
- Developer removes unexposed resist
- Creates a re-entrant profile
- Typical application: liftoff processes (in acetone), often seen in back end processing
- Rule of thumb: resist thickness should be 3x thickness of layer to be lifted off
- Not a standard front end material, but not inherently incompatible with it





Details that matter for lithographic processing



- Existing topography: if your existing feature heights are comparable to or greater than the thickness of the resist that you are putting down, you will not have good coverage
 - Incompletely covered sidewalls, holds full of resist, resist that never enters a hole at all
 - Solutions: eliminate the topography, thicker resist, alternate coating technology (spray on, electrophoretic resist?), use of a previously patterned hard mask instead of a resist mask
- Patterned resist does not have a square profile – can affect the topography of whatever you pattern with the resist
- Resist adhesion
 - If the surface of the wafer is hydrophilic (like SiO_2), the resist might peel during subsequent wet processing steps.
 - Surface preparation is key (e.g. dehydration bake and HMDS coating to render surface hydrophobic)



Cleaning!



- When we say (for example) that positive thin resist is compatible with front end processing, we do not mean that you can have resist on your wafer during most of the front-end process!
- Must remove resist and clean wafer thoroughly before any high temperature processes
- Always include cleaning in process flows, starting at the crayon engineering level
- Resist removal techniques
 - O₂ plasma ash
 - Chemical removal of organics: piranha clean or nanostrip
 - Solvents (acetone)



More cleaning!



Additional cleans typically needed at specified points in the flow

Example: RCA clean before very high temperature processing (as in furnace for front end processing)

- **Step 1: Organic clean, 5:1:1 H₂O:H₂O₂:NH₄OH at 75 - 80C**
- **Step 2: Thin oxide removal, 50:1 H₂O:HF**
- **Step 3: Metal/ionic contamination removal, 6:1:1 H₂O:H₂O₂: HCl at 75 – 80C**

Example: remove organics before moderately high temperature, fairly clean processing (upper part of back end processing)

- **Piranha clean (3:1 H₂SO₄:H₂O₂)**

Materials compatibility (what cleans your structures can tolerate) often determine what processes you can and can't use

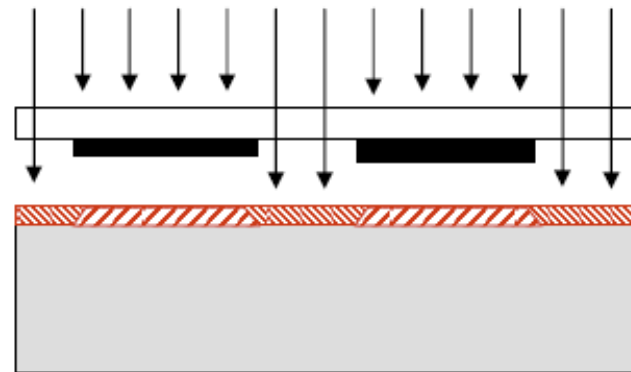
If you wait until the last minute to put cleans into your process flow, you will likely be redesigning your device and process at the last minute



Another important detail: process bias



- The feature drawn on the mask is NOT the same size as the feature produced on the wafer
- Exposed area usually extends beyond clear area on mask
- Resist selection impacts process bias
 - Resist thickness
 - Resist Tone

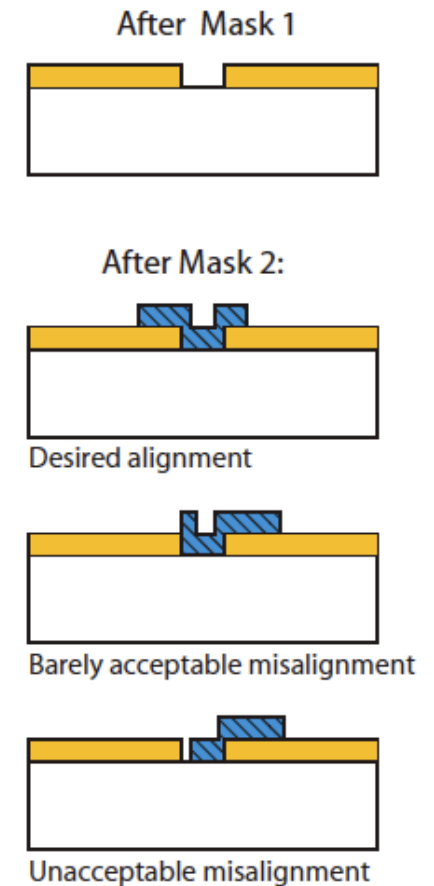
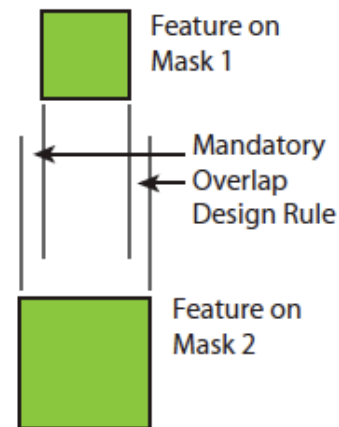




Design Rules



- Alignment of one pattern to the next is critical to device fabrication
- Design rules are created to assure that fabrication tolerances do not destroy devices





Microfabrication Outline

- Substrates – Si, SOI, Fused quartz, etc..
- Lithography and patterning
- Doping
- Thin Films
- Etching
- Wafer Bonding
- Surface Micromachining
- Process Integration



Doping



- Doping is the introduction of a controlled amount of impurities to change the conductivity type and degree of a semiconductor
- In silicon, boron is a p-type dopant (creating holes), while phosphorus, arsenic, and antimony are n-type dopants (creating conduction electrons)
- Some doping incorporated in initial silicon melt
- All modern thin film doping is done with ion implantation
- Doping doesn't add a new thin film, but it modified the properties of a thin film at the surface of an existing material



Ion Implantation



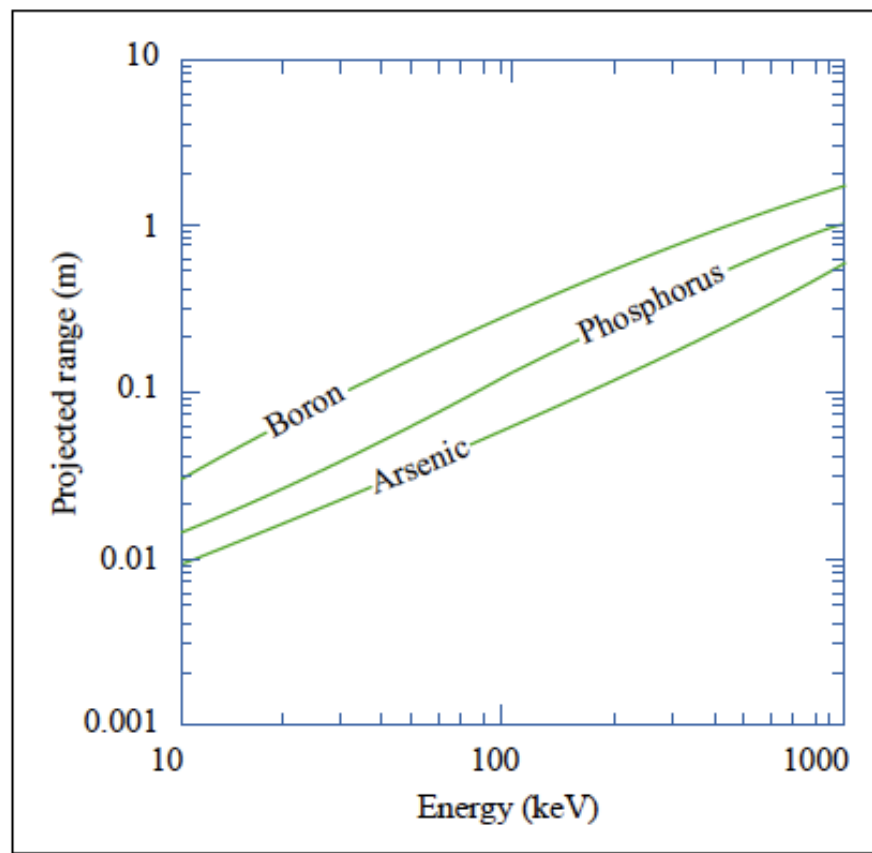
- A high-voltage accelerator is used to shoot ions at the wafer
- The beam must be rastered and the wafer must be rotated to achieve uniform dose
- Usually a thin protective layer, such as oxide, is used to prevent sputtering of the surface and to reduce channeling
- The depth of the implant dose depends on energy
- Activation anneal after implantation allows dopants to reach proper positions in crystal



Effective Range



- The effective range measures the location of the peak concentration of an implanted species

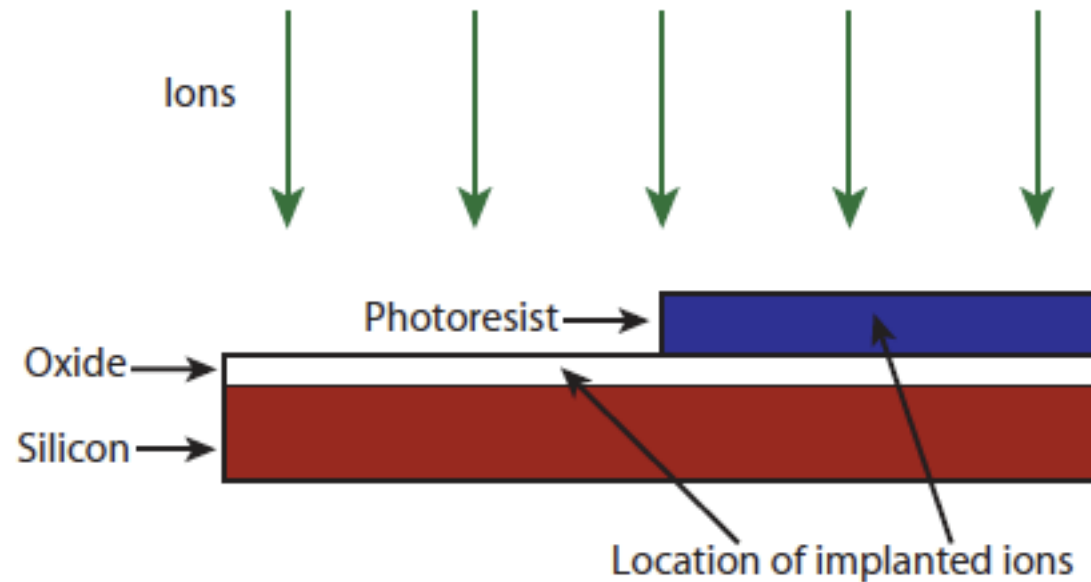




Masking of implants



- Control of which regions of a wafer receive the implant is achieved with masking layers





Diffusion



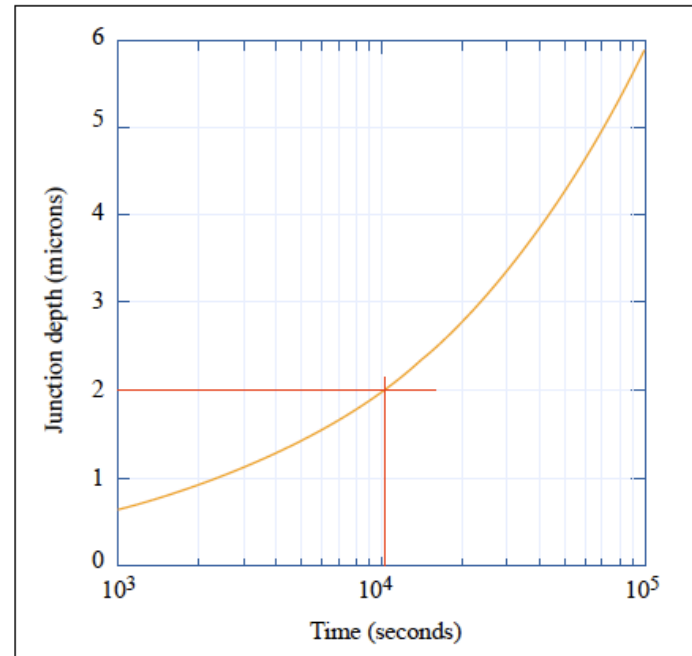
- After implantation, ions are driven deeper into the substrate by diffusion, a high-temperature process
- The junction depth is the point at which the implanted ion concentration is equal (but of opposite type) to the substrate doping

$$x_j = \sqrt{(4Dt) \ln \left(\frac{Q}{N_D \sqrt{\pi Dt}} \right)}$$

Implant dose

Background doping concentration

Image by MIT OpenCourseWare.





Microfabrication Outline

- Substrates – Si, SOI, Fused quartz, etc..
- Lithography and patterning
- Doping
- **Thin Films**
- Etching
- Wafer Bonding
- Surface Micromachining
- Process Integration



Creating thin (and thick) films



- Many techniques to choose from
- Differences:
 - Front or back end processes
 - Quality of resulting films (electrical properties, etch selectivity, defects, residual stress)
 - Conformality
 - Deposition rate, cost
- Physical techniques
 - Material is removed from a source, carried to the substrate, and dropped there
- Chemical Techniques
 - Reactants are transported to the substrate, a chemical reaction occurs, and the product deposit on the substrate to form the desired film



Taxonomy of deposition techniques



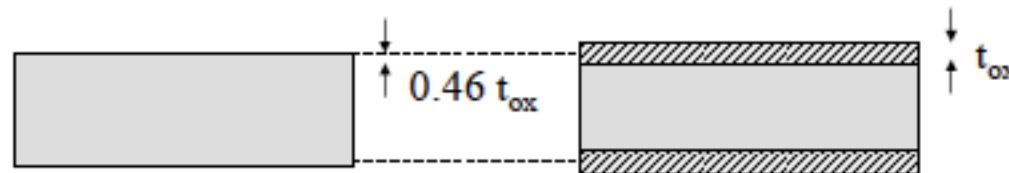
- Chemical
 - Thermal Oxidation
 - Chemical Vapor Deposition (CVD)
 - Low Pressure (LPCVD), Atmospheric pressure (APCVD), Plasma Enhanced (PECVD)
 - Epitaxy
 - Electrodeposition (Electroplating)
- Physical
 - Physical Vapor Deposition (PVD)
 - Evaporation
 - Sputtering
 - Spin-casting



Oxidation I



- Silicon forms a high quality, stable oxide
 - How it works:
 - Oxygen diffuses through oxide to Si/oxide interface
 - $\text{Si} + \text{O}_2 + \text{high temperature } (\sim 1100) \text{ furnace} \rightarrow \text{SiO}_2$
 - Some Si is consumed



- Rate determined by diffusion of oxygen through oxide
- Diffusion limits practical oxide thickness to $< 2 \text{ } \mu\text{m}$
- A key front end process



Oxidation II



- Dry Oxidation (O_2)
 - High quality, slow oxidation rate, smaller maximum thickness (i.e. gate oxide)
- Wet Oxidation (steam)
 - H_2 to speed the diffusion
 - Lower quality, faster oxidation rate
- The Deal-Grove model describe the kinetics of oxidation quite well for oxides greater in thickness that about 30nm



The Deal-Grove Model



For oxides greater than about 30 nm thick:

$$x_{final} = 0.5 \left[A_{DG} \left[\sqrt{1 + \frac{4 B_{DG}}{A_{DG}^2} (t + \tau_{DG})} - 1 \right] \right]$$

where

$$\tau_{DG} = \frac{x_i^2}{B_{DG}} + \frac{x_i}{B_{DG} / A_{DG}}$$

(Constants are given in the text; beware units of B_{DG} , $\mu\text{m}^2/\text{hour}$)

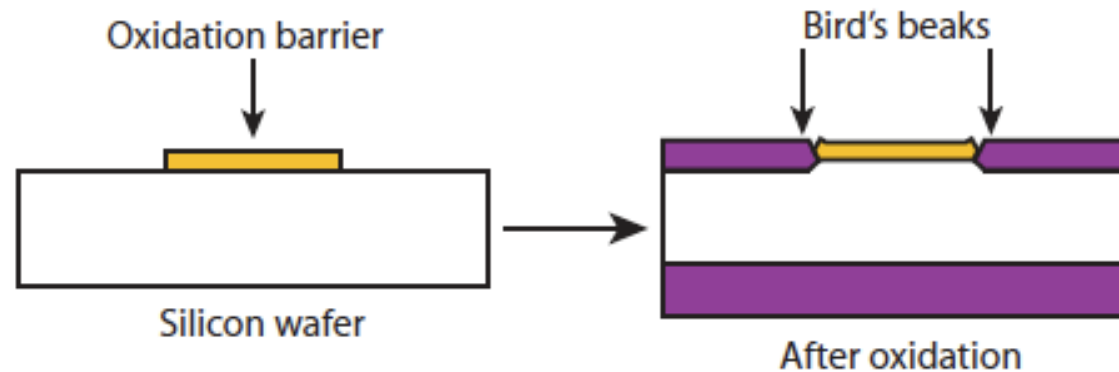
Growth goes approximately as t for short times, and approximately as \sqrt{t} for long times.



Local Oxidation



- Oxidation can be masked locally by an oxidation barrier, such as silicon nitride
- Oxide undercuts edge of mask layer to form a “bird’s beak”
- Oxidation followed by an oxide etch can also be used to sharpen silicon features



Senturia, Microsystem Design.



Chemical Vapor Deposition (CVD)



- How CVD works:
 - Gaseous reactants, often at low pressure
 - Long mean free path; reactants reach substrate
 - Reactants react and deposit products on the substrate
 - Unlike Oxidation, does not consume substrate material
- Energy sources facilitate CVD reactions:
 - High temperature, plasma, laser
- Processing temperatures vary widely
- Commonly deposited films: Oxide, silicon nitride, polysilicon
- CVD results depend on pressures, gas flows, temperature
 - Film composition, uniformity, deposition rate, and electrical and mechanical characteristics can vary



Some reasons to use CVD



- Oxide formation:
 - To get a thicker layer than thermal oxidation can provide
 - To create oxide on a wafer that can't withstand high temperatures (for example because of metal features)
 - To create oxide on top of a material that is not silicon
- For film formation in general
 - To tailor the film properties (like form stress) by adjusting pressures, flow rates, external energy supply, ratios of different precursor gases (to adjust proportions of different materials in the final product)
 - Conformailty : (more or less) even coating on all surfaces
- Drawbacks:
 - Films deposited at low temperature are often lower quality than high temp versions, and have less predictable properties
 - Flammable, toxic or corrosive source gases



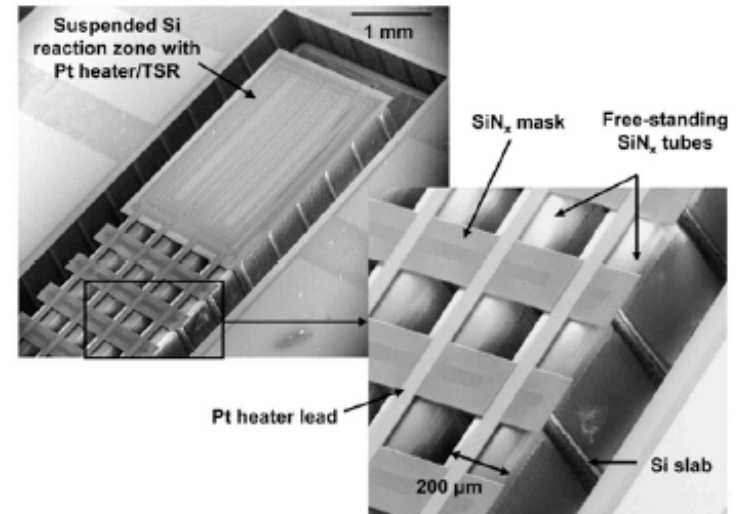
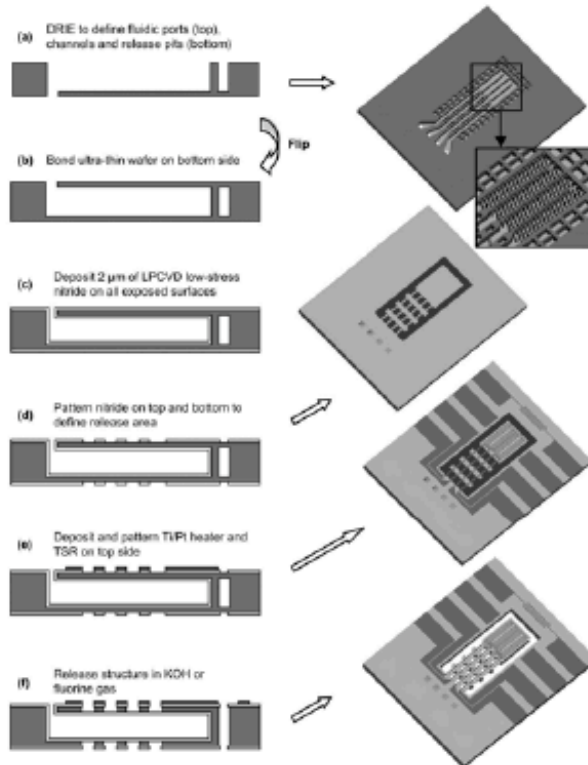
Thick Film Formation



- CVD is a common MEMS tool for creating thick films on the wafer surface
 - In practice, film stress limits thickness (film delamination or cracking, or curvature of underlying structures)
 - Can deposit thick oxides; nitrides are still typically submicron
 - Must anneal deposited oxides for some applications – lose low stress property on anneal



CVD enables conformal coating



MEMS-based fuel processor.



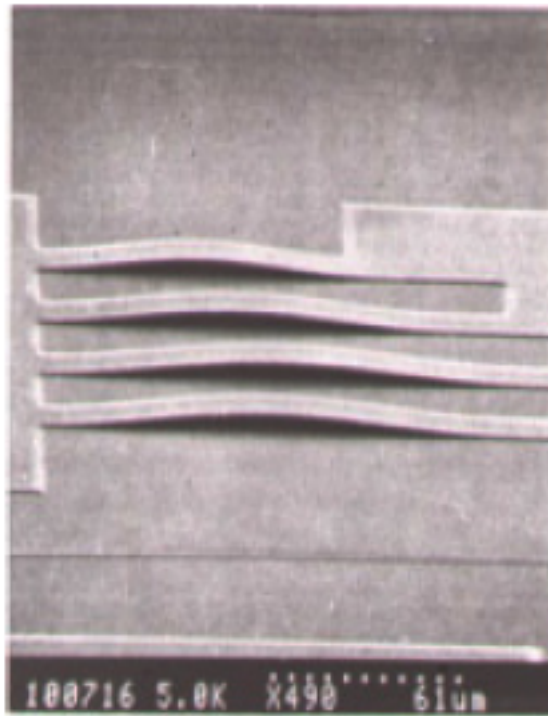
LPCVD Polysilicon



- Amorphous at lower deposition temperatures and high deposition rates
 - Typical temperature: ~590 C
- Polycrystalline at higher deposition temperatures and lower deposition rates
 - Typical temperature: ~625 C
- Grain size and structure depend on detailed deposition conditions
 - E.g. thicker films → larger grains
- Structure, electrical properties, and mechanical properties also vary with post-deposition thermal processing
 - Grain growth
 - Dpoant activation or diffusion



Polysilicon stress depends on deposition rates





Epitaxy



- CVD deposition process in which atoms move to lattice sites, continuing the substrate's crystal structure
 - Homoepitaxy: same material, i.e. Si on Si
 - Heteroepitaxy: different materials, i.e. AlGaAs, on GaAs
- How it happens
 - Slow deposition rate (enough time to find a lattice site)
 - High Temperature (enough energy to move a lattice site)
- Selective epitaxy is possible through masking
- Can grow a doped Si layer of known thickness



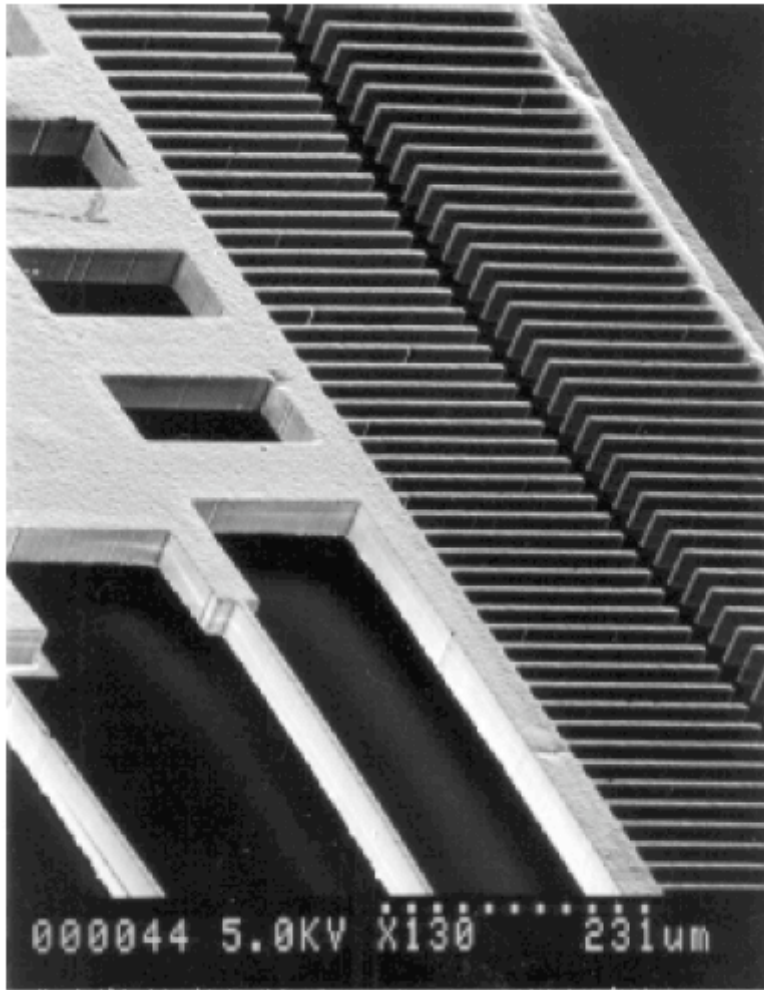
Electroplating: basics



- Pass a current through an aqueous metal solution
 - Anode is made of the meta that you want to deposit
 - Cathode is the conductive seed material on your wafer
 - Positive metal ions travel to the negatively charged cathode on your wafer and deposit there
- Preparing your wafer
 - If you want to plate metal in some places and not in others, you will need a patterned metal seed layer (and typically a “sticky” metal adhesion layer under that)
 - For very short features, just plate onto the seed layer
 - For taller features, need to plate into a mold
 - Molds can be photoresist, silicon, SU-8, et.. Depending on the needs of your device



Electroplating

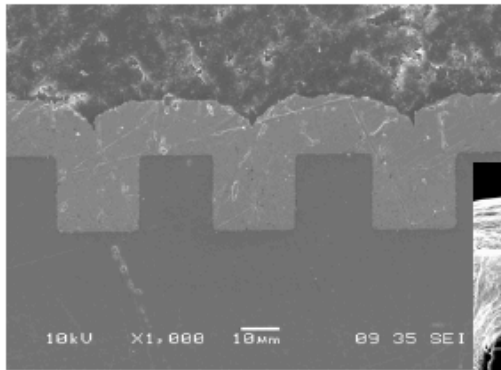


Electroplating for LIGA

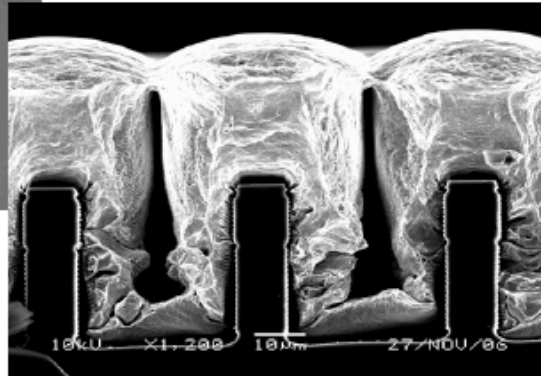
40 μm thick films of nickel fabricated by electroplating into a mold



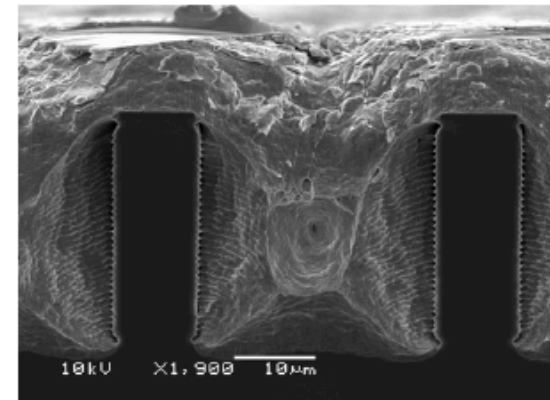
Electroplating realities



Test run w/ bump plating - perfect



Real device forms keyholes – different loading pattern



Solution: Cu damascene fill, with additives/agitation to promote fill at bottom

Courtesy of Dariusz Golda. Used with permission.

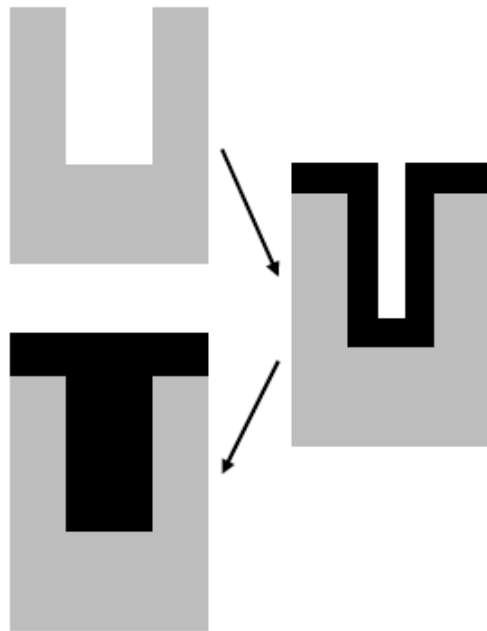


Conformality and keyholes

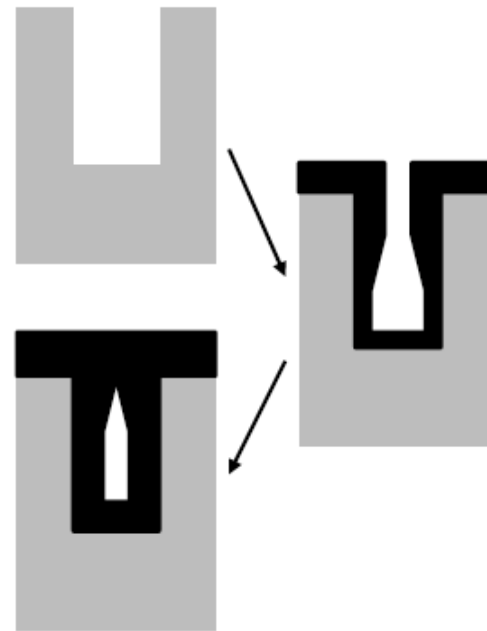


- To lowest order, conformal films coat sidewalls and horizontal surfaces at the same rate
- But high aspect ratio trenches are prone to keyholes (CVD, electroplating, etc..)

What you want:



What you get:



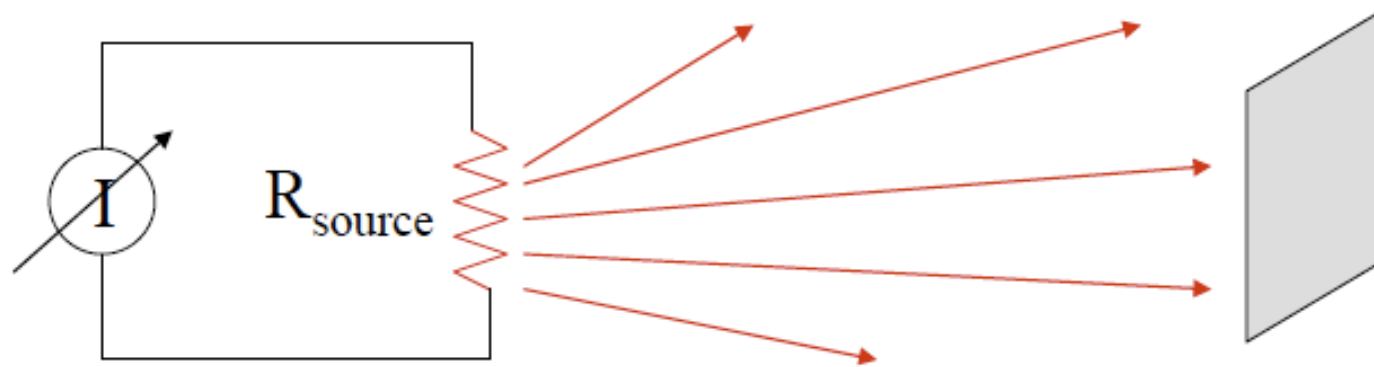


Physical Vapor Deposition

- Remove materials from a solid source
- Transport material to substrate
- Deposit material on substrate
- Differences among PVD techniques
 - How material is removed from source
 - Directionality when it arrives at substrate
 - Cleanliness of deposition
- A family of quick, low temperature processes



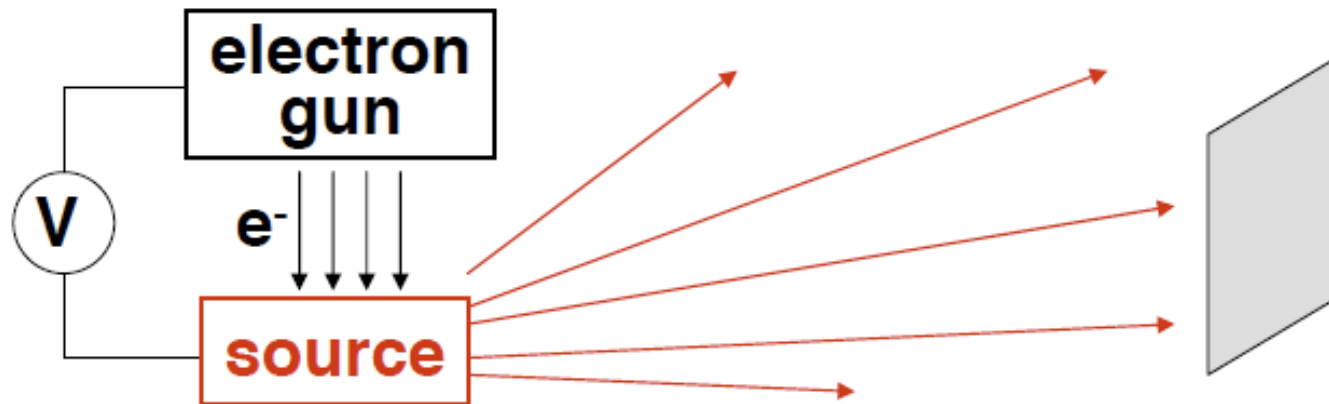
Thermal Evaporation



- Source is resistively heated in high vacuum
 - Typical source: metal
- Hot source atoms are emitted in all directions and stick where they land
- Substrate receives a directional flux of source material
 - Good for liftoff processes, otherwise poor conformality
- Possible contamination from generalized heating



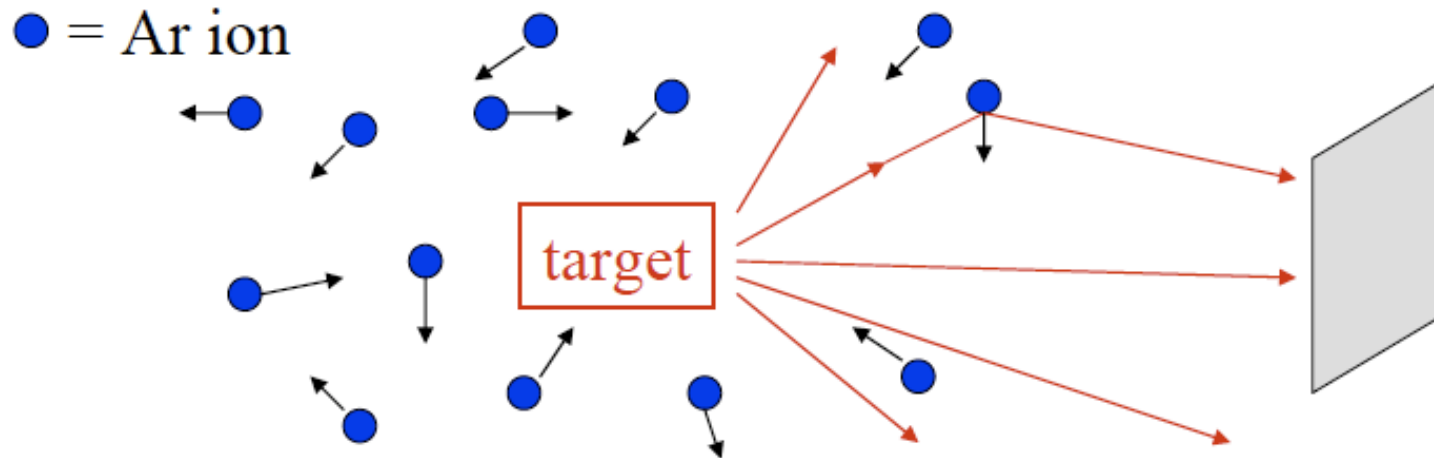
E-beam Evaporation



- Electron beam heats source in high vacuum
 - Typical source: metal
- Hot source atoms are emitted in all directions and stick where they land
- Substrate receives a directional flux of source material
 - Good for liftoff processes, otherwise poor conformality
- Heating is less generalized → less contamination



Sputtering



- Unreactive ions (i.e. Ar) knock material off a target by momentum transfer
- Targets: metals, dielectrics, piezoelectrics, etc..
- Different methods of obtaining energetic ions
 - Magnetron, plasma
- Low pressure, but not high vacuum
- Less directional and faster than evaporation



Etching, liftoff, and adhesion layers



- Films are patterned differently depending on whether the material in question tends to react with other materials
- Materials that react (for example, aluminum):
 - Deposit a blanket film (sputtering good for better conformality), do photolithography, and etch it into desired shape
- Materials that don't react readily (for example, noble metals):
 - Hard to etch: typically use liftoff instead
 - Pattern resist, then deposit metal on top with a directional deposition tool
 - Not very sticky: typically need an adhesion layer to stick the noble metal to what lies beneath
 - Example: use a few hundred Å thick layer of Cr or Ti to adhere Au to an underlying oxide (deposited without breaking vacuum between layers)



Is that all you can do with deposited films?



- No!
- Spin-casting: put the stuff that you want to deposit in a liquid, spin it onto the surface like resist, and bake out the solvent (spin on glass, PZT piezoelectrics)
- Other forms of vapor deposition designed for a particular purpose (depositing the inert polymer parylene by vapor deposition followed by polymerization)
- Lamination of free-standing resist films onto surfaces
- Self assembled monolayers
- ...



Microfabrication Outline



- Substrates – Si, SOI, Fused quartz, etc..
- Lithography and patterning
- Doping
- Thin Films
- Etching
- Wafer Bonding
- Surface Micromachining
- Process Integration



Etching



- Wet Etching
 - Isotropic
 - Anisotropic (for crystals only)
- Dry etching using plasma reactors
 - Isotropic “plasma” etching at relatively high gas pressures
 - Anisotropic “reaction-ion” etching at relatively lower gas pressures
- Sputter etching or ion-beam milling
 - Not very selective
- A useful reference (what etches what and how fast):
 - Williams, Gupta, and Wasilik, “Etch Rates for Micromachining Processing – Part II”, JMEMS 12, 761-778 (2003).



Considerations for etching



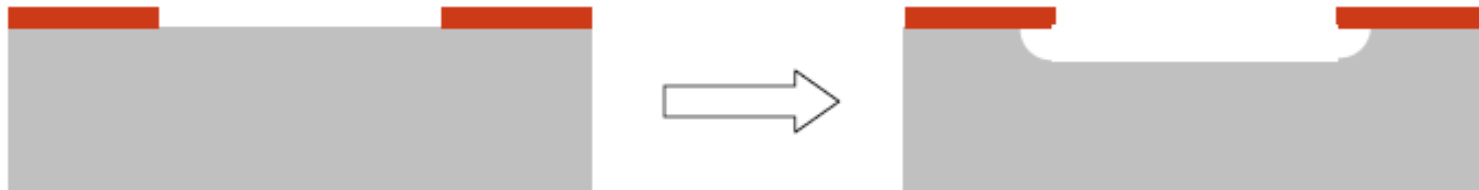
- **Isotropic**
 - Etch rate the same in all crystal directions
- **Anisotropic**
 - For wet etches, rate depends on crystal plane
 - For dry etches, directionality determined by process
- **Selectivity**
 - Etch rate of substrate vs. etch rate of mask
- **Mask Adhesion (for wet etching)**
 - Increased etching along mask/substrate interface
- **Temperature**
 - Reaction rate limited?
- **Stirring**
 - Mass transfer limited?



Isotropic Etching



- Etch rate is independent of orientation
- Isotropic etch profile
 - Assume a well-adhered mask with infinite selectivity
 - Mask undercut, rounded etch profile



- Applications
 - Flow channels
 - Removal of sacrificial layers in surface micromachining



Isotropic etching



- Some wet etches:
 - Si mixture of nitric, acetic, and HF
 - SiO₂ buffered HF (BOE), also HF vapor
 - SiN hot phosphoric acid
 - PolySi KOH
 - Al PAN etch (phosphoric, acetic, nitric acids)
- Some dry etches:
 - Si XeF₂ vapor
 - Organics O₂ plasma
- Mostly clean enough for front end, with the exception of KOH, which is a contamination risk for very high T processes. XeF₂ vapor is often used as a final release etch



Anisotropic wet etching



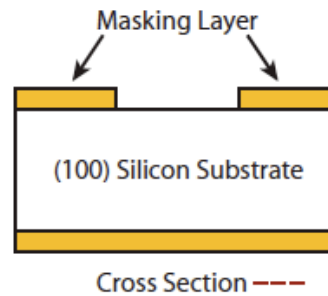
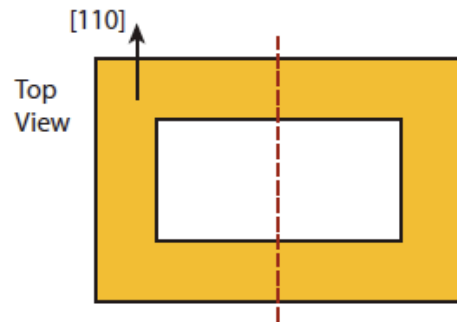
- Depends on having a single-crystal substrate
- The effect depends on the different etch rates of different exposed crystal planes
- Silicon etchants for which $\langle 111 \rangle$ planes etch slowly
 - Strong bases (KOH, NaOH, NH_4OH)
 - TMAH
 - Ethylene diamine pyrochatechol
 - Hydrazine



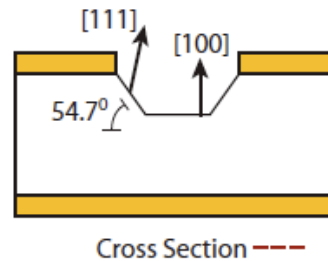
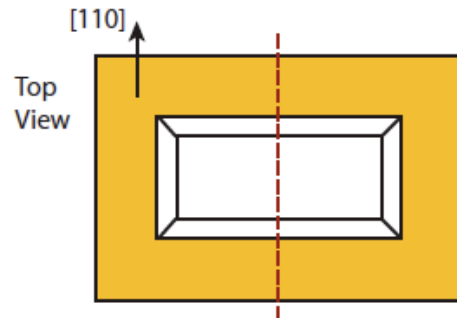
Making a Trench with KOH



Before Etching



After Etching



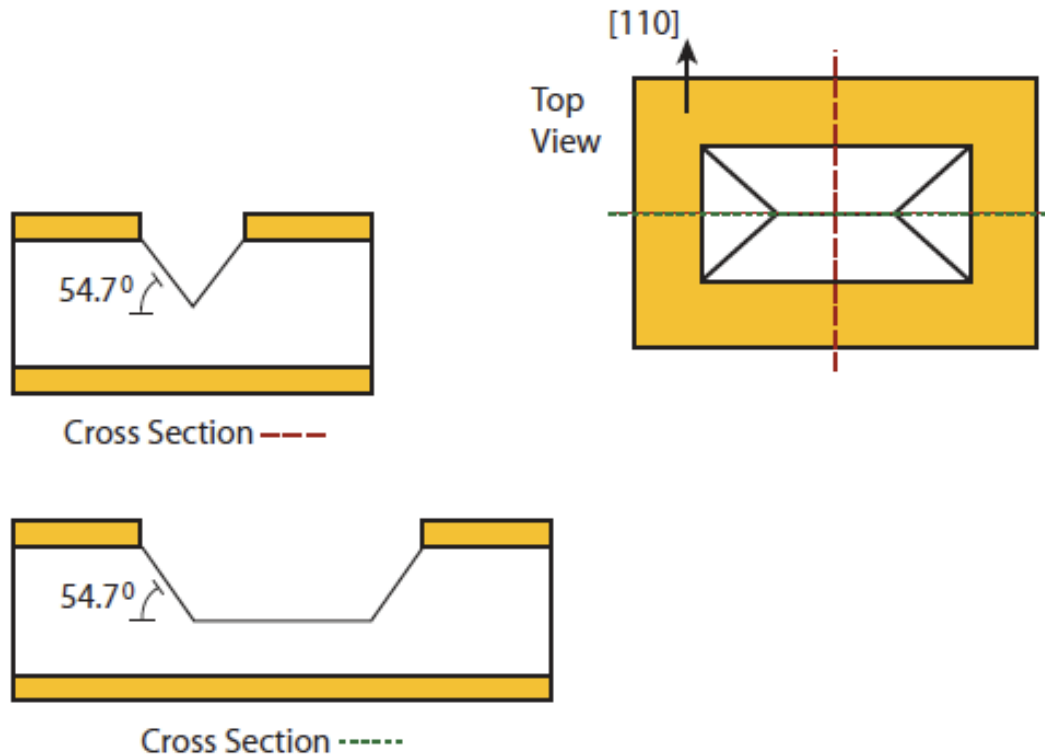
- A rectangular patten is aligned to a $[110]$ direction on a $\langle 100 \rangle$ silicon wafer



Making a V-groove



- The previous etch is allowed to go to “termination”, i.e. the slowing of etch rate with only $\{111\}$ planes are exposed (can also make square, pyramidal)

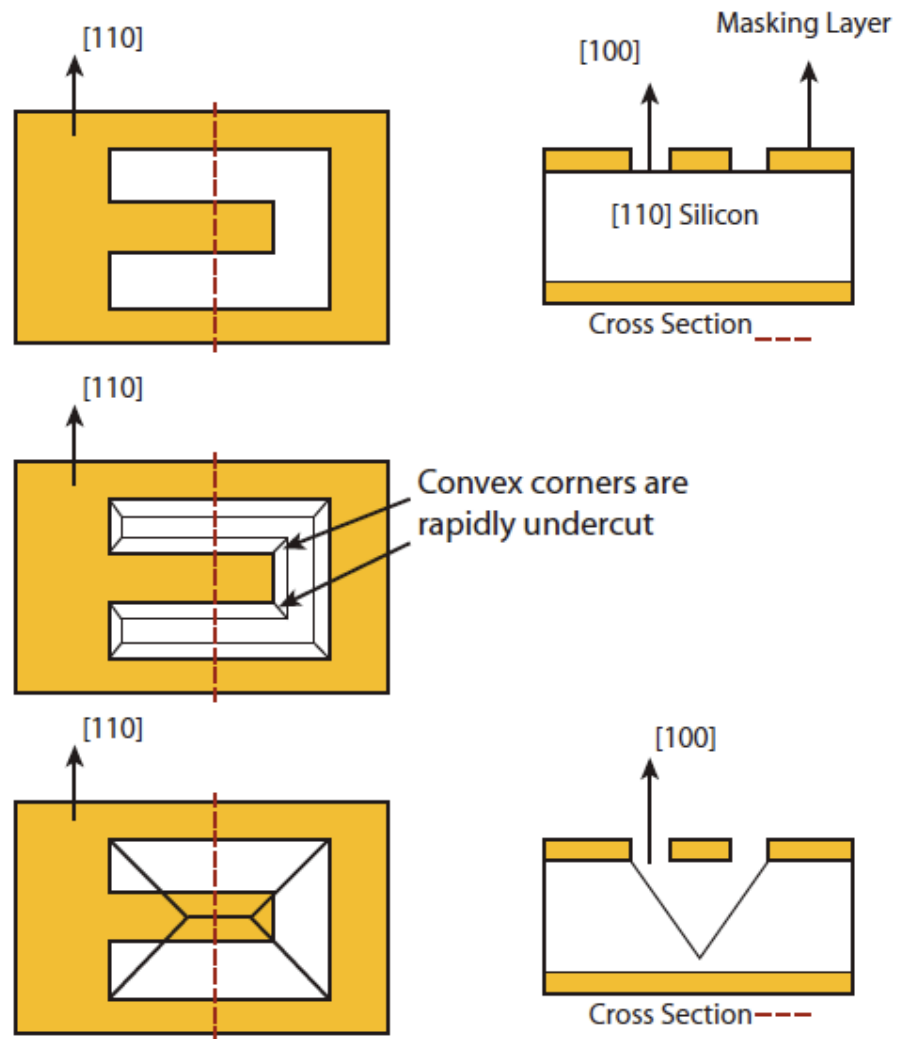




Convex Corners

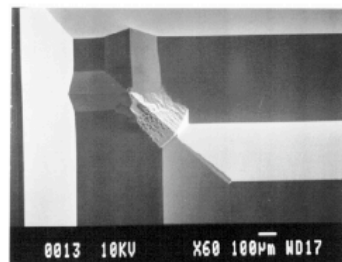
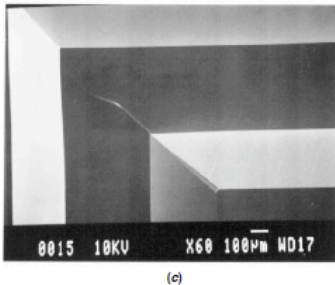
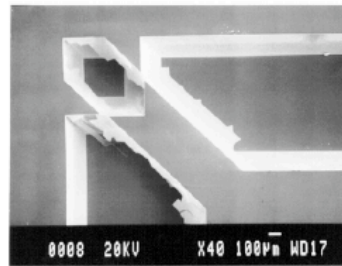
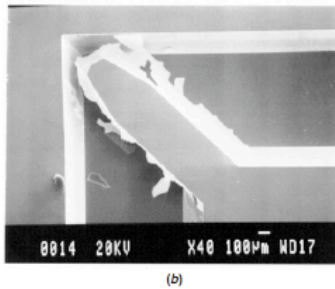
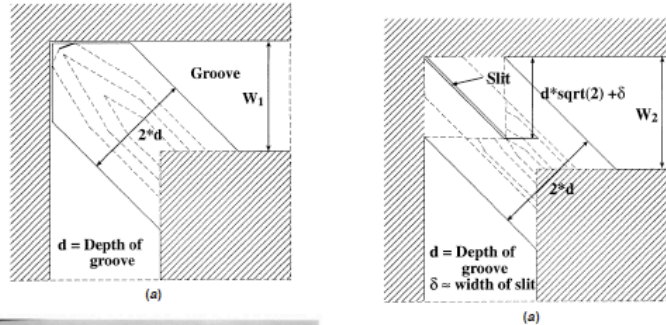


- Convex corners become undercut, as there is no single slow-etching (111) plane to stop on





Corner Compensation



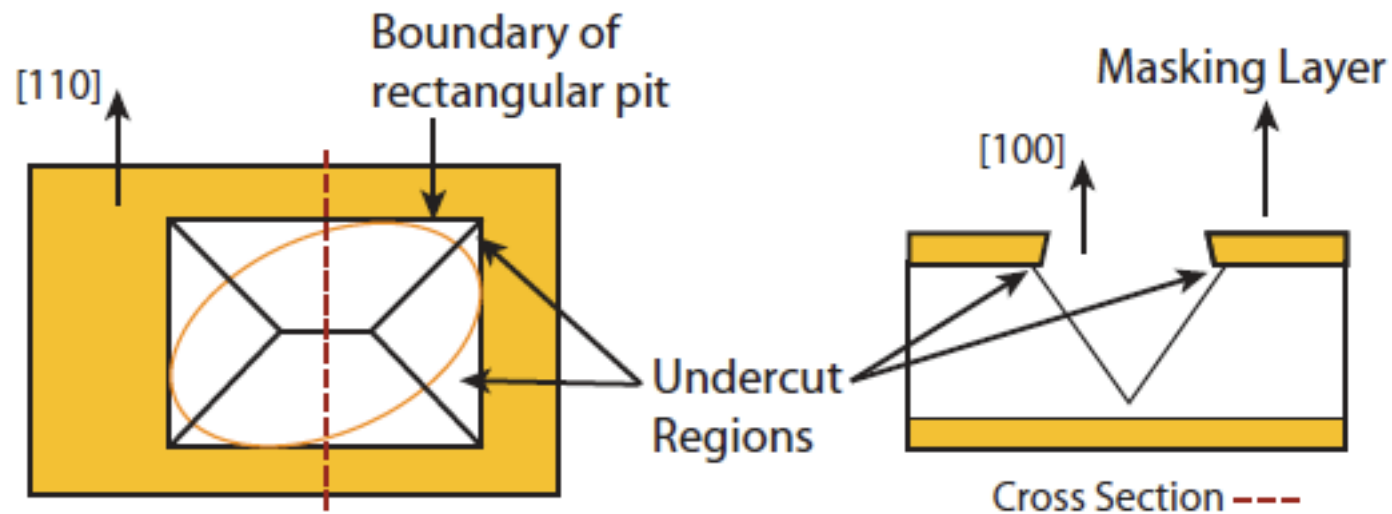
- To etch a convex corner with KOH, add extra material at corner
- Amount of material is chosen so that it will etch away just when the overall etch reaches the desired depth
- Extra material protect convex corner from attack



Arbitrary Shapes



- Any mask feature, if etched long enough, will result in a V-groove tangent to the mask along $\langle 110 \rangle$ directions

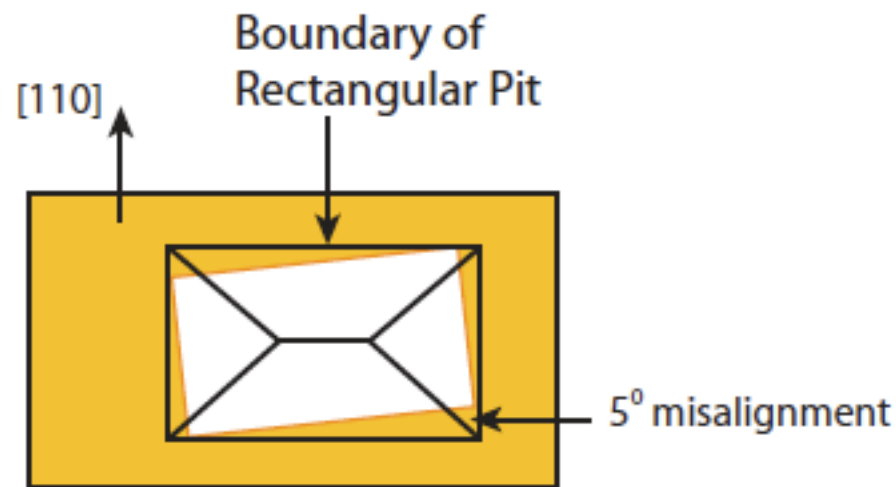




Misalignment



- Misalignment of the mask relative to the $[110]$ direction always results in a larger etched region





Selectivity and etch masks for KOH etches



- Deep etches are long – selectivity matters
- Mask must last long enough to bring the etch to completion
- Sidewall erosion must be at an acceptably slow rate
- Etch rate of $\{111\}$ planes is finite but small
 - Condition-dependent, of order 400:1 for $\{100\}$ rate/ $\{111\}$ rate
- Etch rate of mask
 - Si:SiO₂ selectivity about 100:1
 - Si:LPCVD SiN selectivity at least 1000:1
 - PECVD SiN not effective (low quality)
 - Do NOT use photoresist!



Etch Stops



- When etching into a wafer to leave a specific thickness of material, it is necessary to have some kind of etch stop
- Example



Dry (Plasma) Etching



- At reduced pressure, a glow discharge is set up in a reactive gas environment
- This produces
 - Ions that can be accelerated by the electric fields at the bounding edges of the plasma so that they strike the surface
 - These can be quite directional in their impact
 - Free radicals (uncharged) that can diffuse to the surface and undergo reaction
- Etching depends on reaction followed by creation of a gaseous byproduct which is pumped away



Applicability



- Most materials can be plasma etched
 - Oxide
 - Nitride
 - Silicon
 - Most Metals (not the noble metals)
 - Polymers
- The art is in achieving suitable selectivity both for masking layers and to layers that lie beneath the layer being etched
 - Known recipes (gas mixtures, plasma conditions) with desired selectivity
 - End-point detection is an important part of “best practice” when using plasma etching



Shape



- The higher the pressure, the more isotropic the etch because reactants are scattered many times before reaching the surface (this is called “plasma etching”)
- To achieve directional anisotropy, one must go to low pressure to achieve long mean-free paths for the ions (this is called “reactive-ion etching” or RIE)
- Deep reactive ion etching is another thing altogether



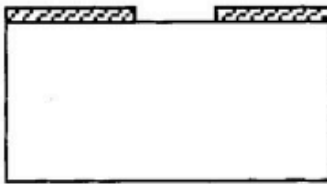
Deep reactive Ion Etching (The Bosch Process)



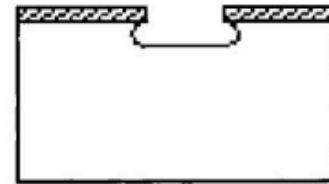
- Photoresist mask: selectivity about 50:1
- Oxide Mask: selectivity > 100:1

•

1. Pattern photoresist



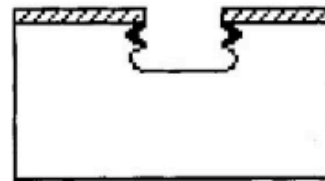
2. Reactive ion etch in SF₆



**3. Deposit passivation (C₄F₈)
(produces a teflon-like polymer)**



**4. Etch and repeat cycle
(directional ions clear passivation
from bottom only)**





Depth depends on features and layout



- Features of difference width etch at different rates (recipe dependent)



Multi-level Etching



- Making multi-level etches can be challenging
- For through etches with two different depths, simply etch from both sides of wafer, with double-sided alignment

Pattern side 1



Etch side 1



**Flip wafer and
pattern side 2**



Etch side 2

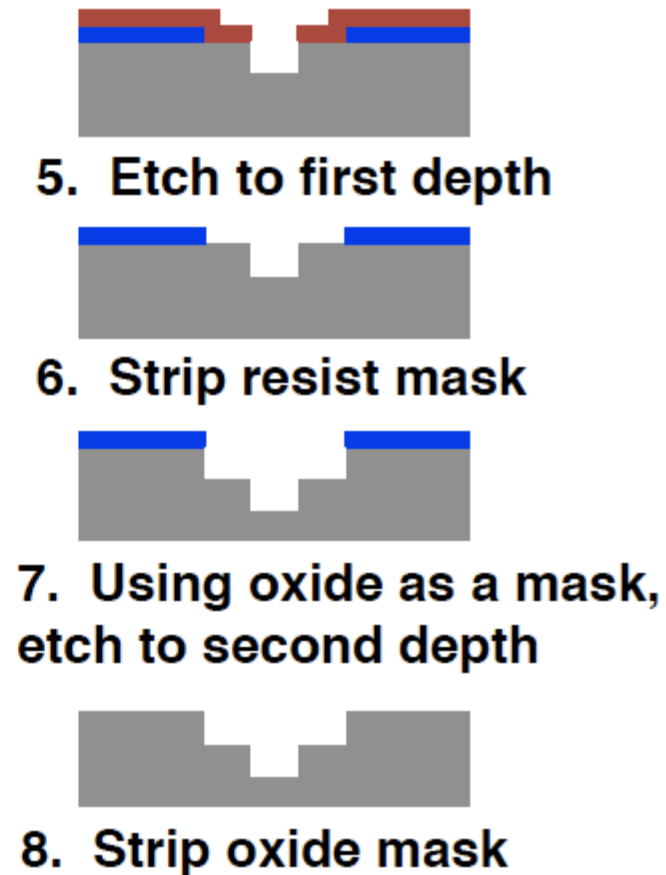
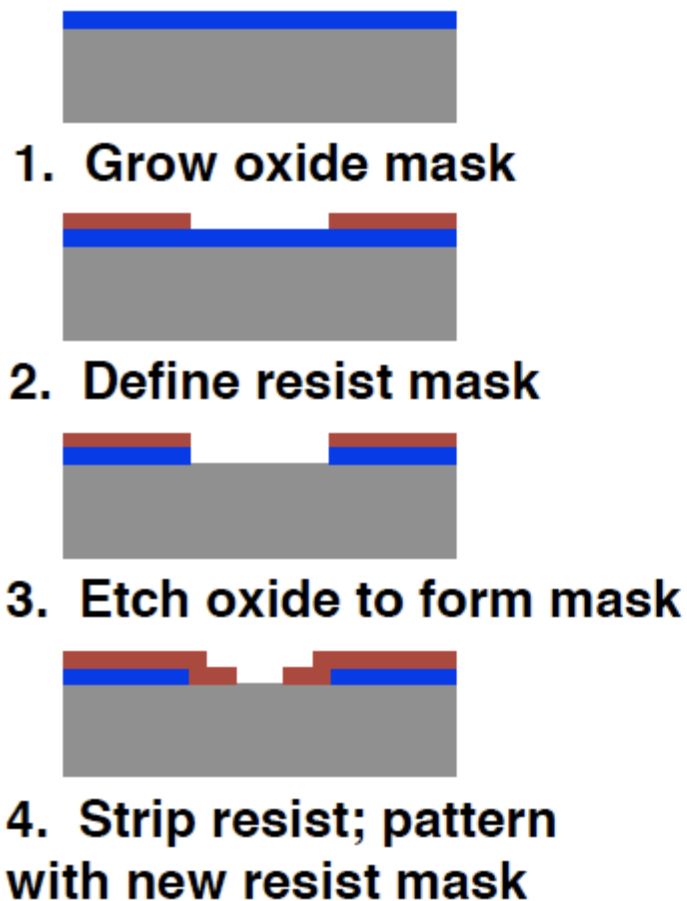




Multi-level etching with nested masks



- Etching two sets of deep (> about 10 μm) features on the same side of the wafer requires a nested mask





DRIE with Etch Stop



- SOI substrate
- Buried oxide acts as an etch stop
- Charging can led to “footing”

