# ME 141B: The MEMS Class Introduction to MEMS and MEMS Design

Sumita Pennathur
UCSB

# Microfabrication Outline

- Substrates – Si, SOI, Fused quartz, etc..
- Lithography and patterning
- Doping
- Thin Films
- Etching
- Wafer Bonding
- Surface Micromachining
- Process Integration

# Creating thin (and thick) films

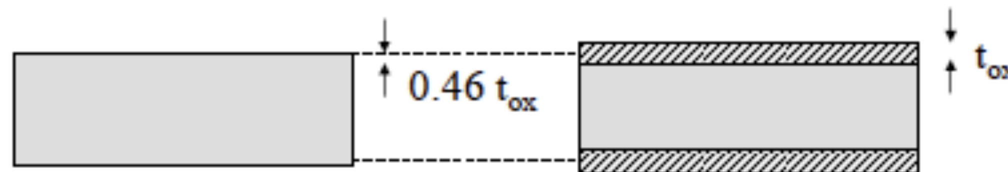
- Many techniques to choose from
- Differences:
  - Front or back end processes
  - Quality of resulting films (electrical properties, etch selectivity, defects, residual stress)
  - Conformality
  - Deposition rate, cost
- Physical techniques
  - Material is removed from a source, carried to the substrate, and dropped there
- Chemical Techniques
  - Reactants are transported to the substrate, a chemical reaction occurs, and the product deposit on the substrate to form the desired film

# Taxonomy of deposition techniques

- Chemical
  - ➢ Thermal Oxidation
  - ➢ Chemical Vapor Deposition (CVD)
    - Low Pressure (LPCVD), Atomspheric pressure (APCVD), Plasma Enhanced (PECVD)
  - ➢ Epitaxy
  - ➢ Electrodeposition (Electroplating)
- Physical
  - ➢ Physical Vapor Deposition (PVD)
    - Evaporation
    - Sputtering
  - ➢ Spin-casting

# Oxidation I

- Silicon forms a high quality, stable oxide
  - ➢ How it works:
    - Oxygen diffuses through oxide to SI/oxide interface
    - SI + $O_2$ + high temperature (~1100) furnace → $SiO_2$
    - Some Si is consumed




  - ➢ Rate determined by diffusion of oxygen through oxide
  - ➢ Diffusion limits practical oxide thickness to < 2 um
  - ➢ A key front end process

# Oxidation II

- Dry Oxidation ($O_2$)
  - High quality, slow oxidation rate, smaller maximum thickness (i.e. gate oxide)
- Wet Oxidation (steam)
  - $H_2$ to speed the diffusion
  - Lower quality, faster oxidation rate
- The Deal-Grove model describe the kinetics of oxidation quite well for oxides greater in thickness that about 30nm

# The Deal-Grove Model

**For oxides greater than about 30 nm thick:**

$$x_{final} = 0.5\left[A_{DG}\left[\sqrt{1+\frac{4B_{DG}}{A_{DG}^{2}}\left(t+\tau_{DG}\right)}-1\right]\right]$$

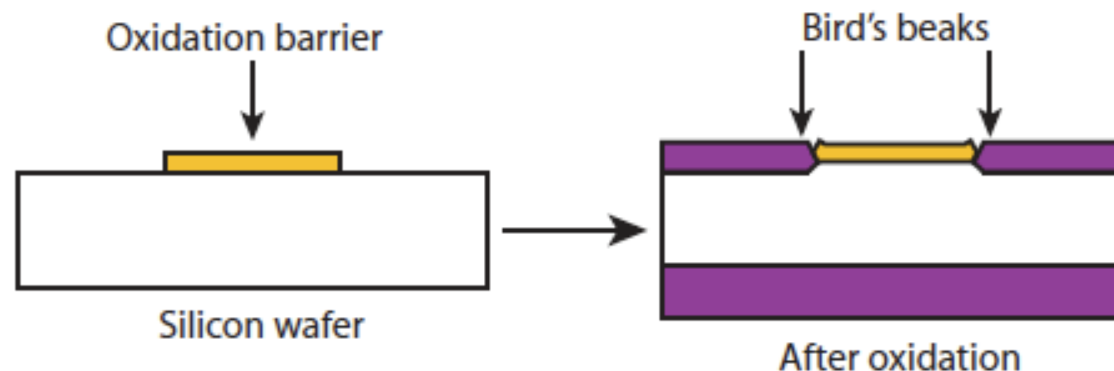
**where** $$\tau_{DG} = \frac{x_i^2}{B_{DG}} + \frac{x_i}{B_{DG}/A_{DG}}$$

**(Constants are given in the text; beware units of $B_{DG}$, μm²/hour)**

**Growth goes approximately as *t* for short times, and approximately as $\sqrt{t}$ for long times.**

# Local Oxidation

- Oxidation can be masked locally by an oxidation barrier, such as silicon nitride
- Oxide undercuts edge of mask layer to form a “bird’s beak”
- Oxidation followed by an oxide etch can also be used to sharpen silicon features




**Senturia, Microsystem Design.**

# Chemical Vapor Deposition (CVD)

- How CVD works:
  - Gaseous reactants, often at low pressure
  - Long mean free path; reactants reach substrate
  - Reactants react and deposit products on the substrate
  - Unlike Oxidation, does not consume substrate material
- Energy sources facilitate CVD reactions:
  - High temperature, plasma, laser
- Processing temperatures vary widely
- Commonly deposited films: Oxide, silicon nitride, polysilicon
- CVD results depend on pressures, gas flows, temperature
  - Film composition, uniformity, deposition rate, and electrical and mechanical characteristics can vary

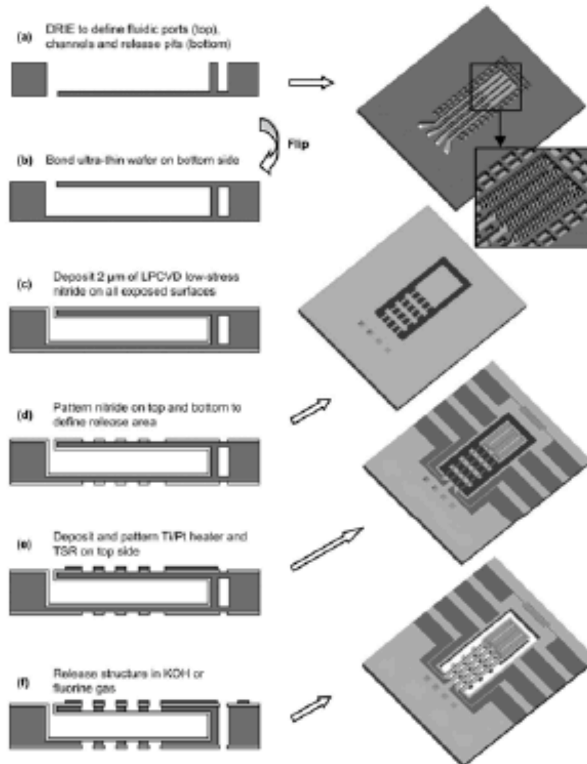
# Some reasons to use CVD

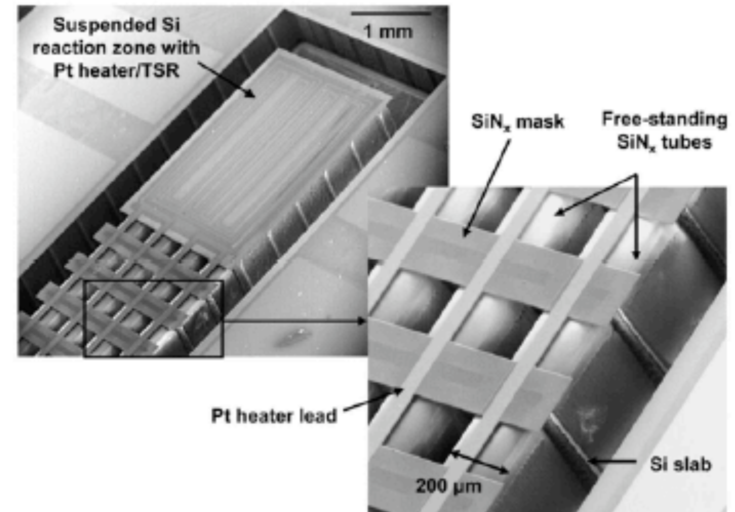
- Oxide formation:
  - To get a thicker layer than thermal oxidation can provide
  - To create oxide on a wafer that can't withstand high temperatures (for example because of metal features)
  - To create oxide on top of a material that is not silicon
- For film formation in general
  - To tailor the film properties (like form stress) by adjusting pressures, flow rates, external energy supply, ratios of different precursor gases (to adjust proportions of different materials in the final product)
  - Conformailty : (more of less) even coating on all surfaces
- Drawbacks:
  - Films deposited at low temperature are often lower quality than high temp versions, and have less predictable properties
  - Flammable, toxic or corrosive source gases

# Thick Film Formation

- CVD is a common MEMS tool for creating thick films on the wafer surface
  - In practice, film stress limits thickness (film delamination or cracking, or curvature of underlying structures)
  - Can deposit thick oxides; nitrides are still typically submicron
  - Must anneal deposited oxides for some applications – lose low stress property on anneal

# CVD enables conformal coating



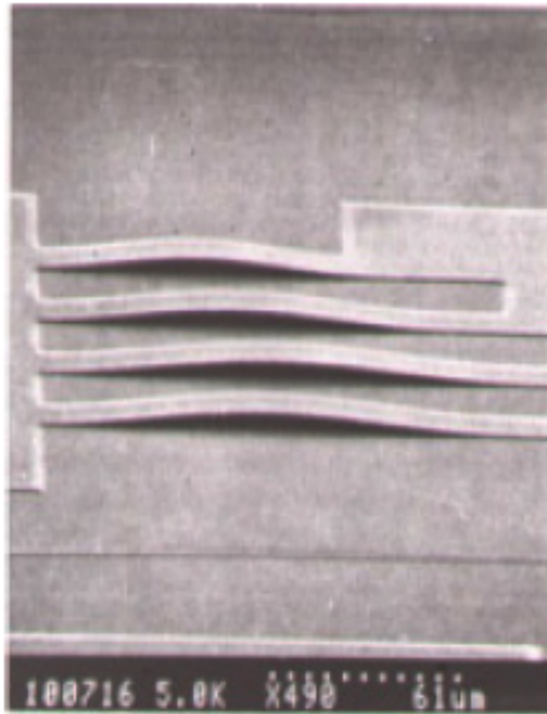




MEMS-based fuel processor.

# LPCVD Polysilicon

- Amorphous at lower deposition temperatures and high deposition rates
  - Typical temperature: ~590 C
- Polycrystalline at higher deposition temperatures and lower deposition rates
  - Typical temperature: ~625 C
- Grain size and structure depend on detailed deposition conditions
  - E.g. thicker films → larger grains
- Structure, electrical properties, and mechanical properties also vary with post-deposition thermal processing
  - Grain growth
  - Dpoant activation or diffusion

# Polysilicon stress depends on deposition rates



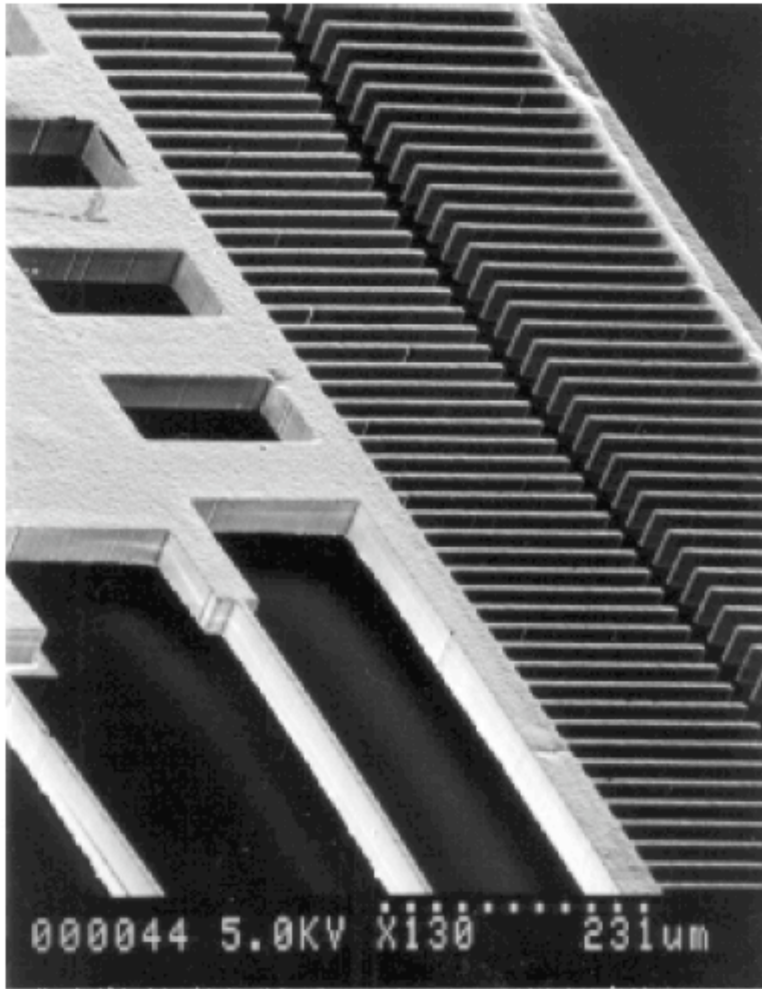
# Epitaxy

- CVD deposition process in which atoms move to lattice sites, continuing the substrate's crystal structure
  - Homoepitaxy: same material, i.e. Si on Si
  - Heteroepitaxy: different materials, i.e. AlGaAs, on GaAs
- How it happens
  - Slow deposition rate (enough time to find a lattice site)
  - High Temperature (enough energy to move a lattice site)
- Selective epitaxy is possible through masking
- Can grow a doped Si layer of known thickness

# Electroplating: basics

- Pass a current through an aqueous metal solution
  - Anode is made of the meta that you want to deposit
  - Cathode is the conductive seed material on your wafer
  - Positive metal ions travel to the negatively charged cathode on your wafer and deposit there
- Preparing your wafer
  - If you want to plate metal in some places and not in others, you will need a patterned metal seed layer (and typically a “sticky” metal adhesion layer under that)
  - For very short features, just plate onto the seed layer
  - For taller features, need to plate into a mold
  - Molds can be photoresist, silicon, SU-8, et.. Depending on the needs of your device

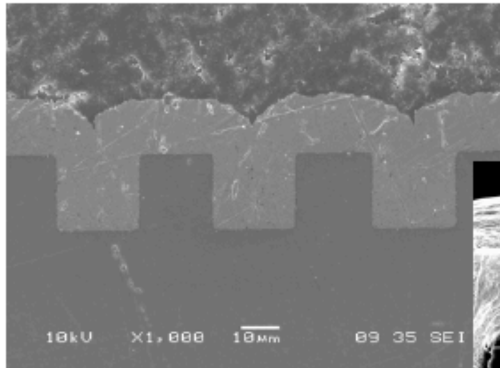
# Electroplating



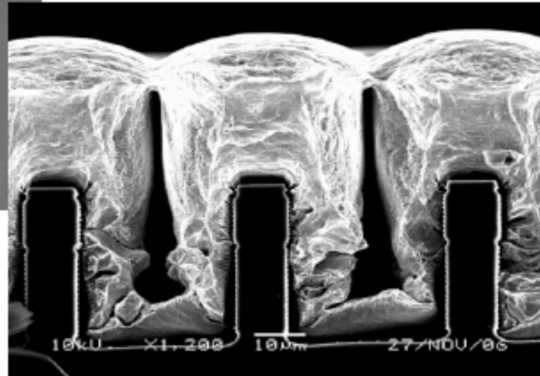

**Electroplating for LIGA**

**40 $\mu$m thick films of nickel fabricated by electroplating into a mold**

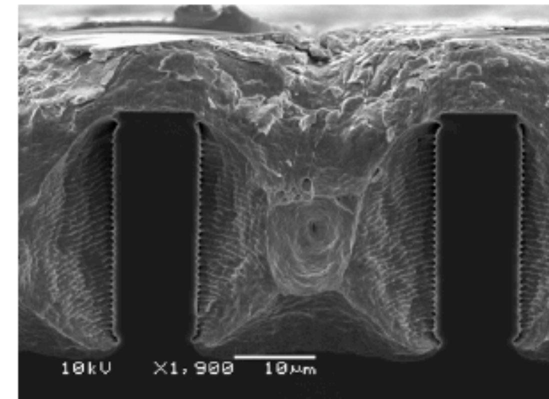
# Electroplating realities




Test run w/ bump plating - perfect



Real device forms keyholes – different loading pattern

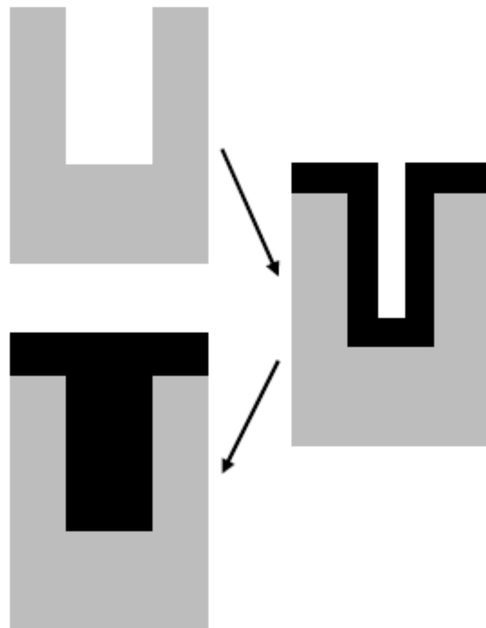


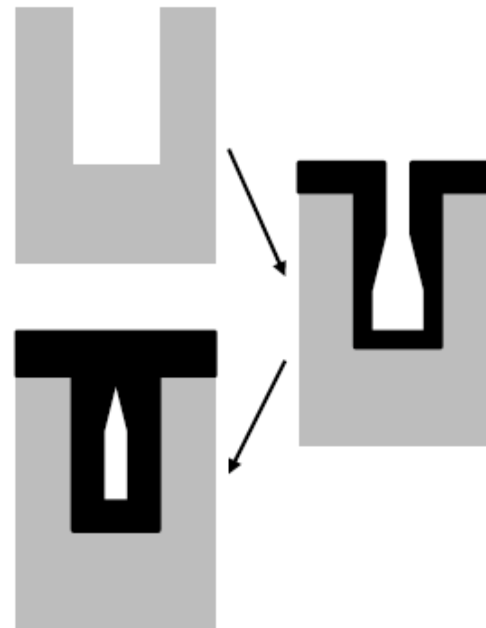

Solution: Cu damascene fill, with additives/agitation to promote fill at bottom

Courtesy of Dariusz Golda. Used with permission.

# Conformality and keyholes

- To lowest order, conformal films coat sidewalls and horizontal surfaces at the same rate
- But high aspect ratio trenches are prone to keyholes (CVD, electroplating, etc..)

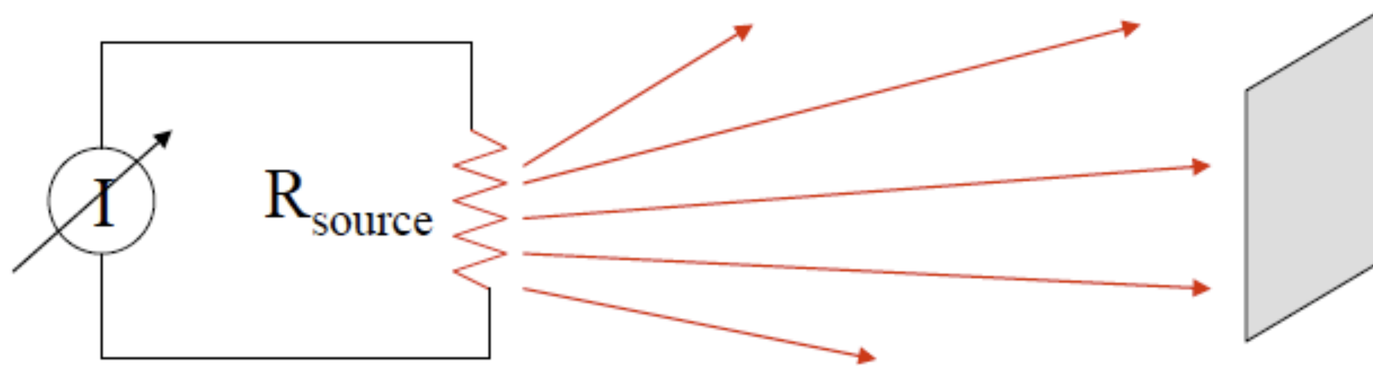


# Physical Vapor Deposition

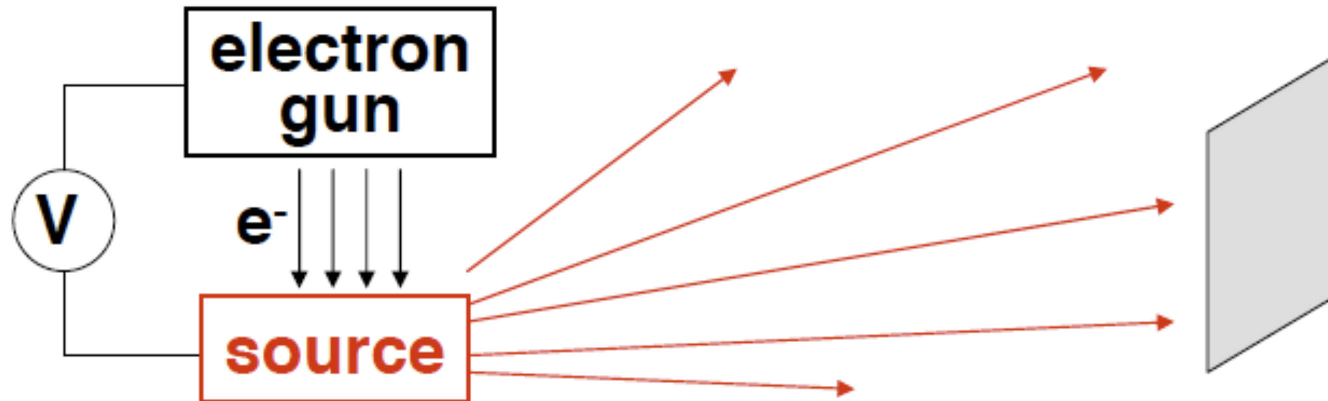
- Remove materials from a solid source
- Transport material to substrate
- Deposit material on substrate
- Differences among PVD techniques
  - How material is removed from source
  - Directionality when it arrives at substrate
  - Cleanliness of deposition
- A family of quick, low temperature processes

# Thermal Evaporation



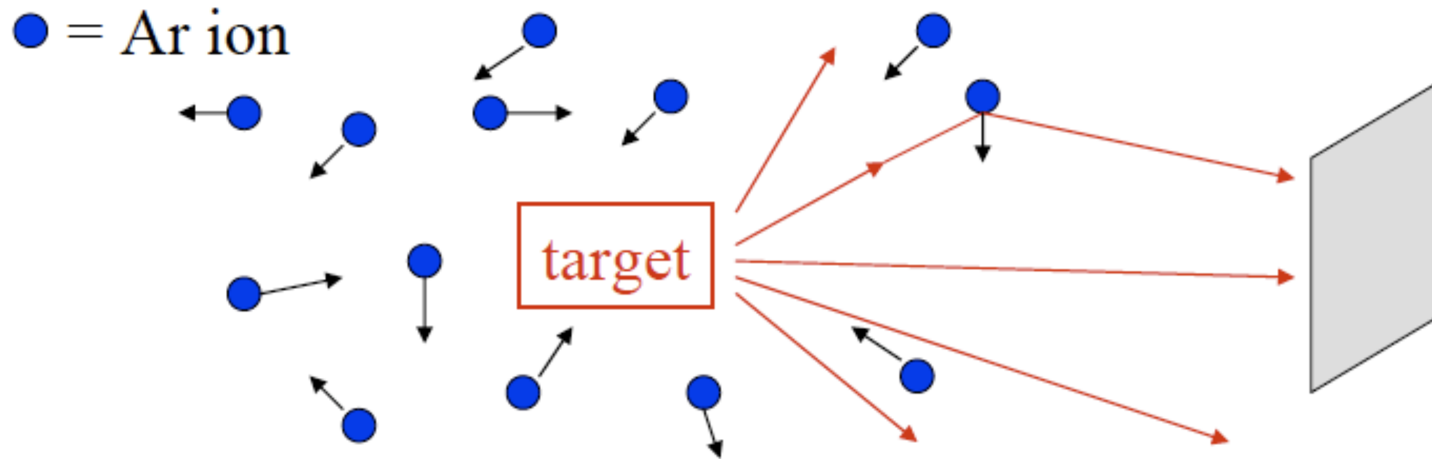

- Source is resistively heated in high vacuum
  - Typical source: metal
- Hot source atoms are emitted in all directions and stick where they land
- Substrate receives a directional flux of source material
  - Good for liftoff processes, otherwise poor conformality
- Possible contamination from generalized heating

# E-beam Evaporation




- Electron beam heats source in high vacuum
  - Typical source: metal
- Hot source atoms are emitted in all directions and stick where they land
- Substrate receives a directional flux of source material
  - Good for liftoff processes, otherwise poor conformality
- Heating is less generalized → less contamination

# Sputtering




- Unreactive ions (i.e. Ar) knock material off a target by momentum transfer
- Targets: metals, dielectrics, piezoelectrics, etc..
- Different methods of obtaining energetic ions
  - Magnetron, plasma
- Low pressure, but not high vacuum
- Less directional and faster than evaporation

# Etching, liftoff, and adhesion layers

- Films are patterned differently depending on whether the material in question tends to react with other materials
- Materials that react (for example, aluminum):
  - Deposit a blanket film (sputtering good for better conformality), do photolithography, and etch it into desired shape
- Materials that don't react readily (for example, noble metals):
  - Hard to etch: typically use liftoff instead
  - Pattern resist, then deposit metal on top with a directional deposition tool
  - Not very sticky: typically need an aehesion layer to stick the noble metal to what lies beneath
  - Example: use a few hundred A thick layer of Cr or Ti to adhere Au to an underlying oxide (deposited without breaking vacuum between layers)

# Is that all you can do with deposited films?

- No!
- Spin-casting: put the stuff that you want to deposit in a liquid, spin it onto the surface like resist, and bake out the solvent (spin on glass, PZT piezoelectrics)
- Other forms of vapor deposition designed for a particular purpose (depositing the inert polymer parylene by vapor deposition followed by polymerization)
- Lamination of free-standing resist films onto surfaces
- Self assembled monolayers
- …

# Microfabrication Outline

- Substrates – Si, SOI, Fused quartz, etc..
- Lithography and patterning
- Doping
- Thin Films
- Etching
- Wafer Bonding
- Surface Micromachining
- Process Integration

# Etching

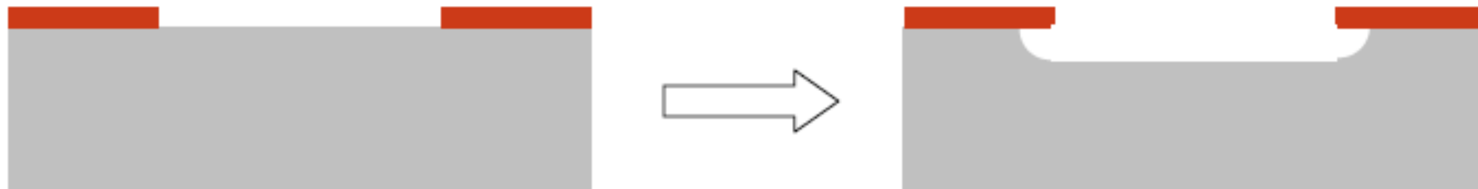
- Wet Etching
  - Isotropic
  - Anisotropic (for crystals only)
- Dry etching using plasma reactors
  - Isotropic “plasma” etching at relatively high gas pressures
  - Anisotrpoic “reaction-ion” etching at relatively lower gas pressures
- Sputter etching or ion-beam milling
  - Not very selective
- A useful reference (what etches what and how fast):
  - Williams, Gupta, an Wasilik, “Etch Rates for Micromachining Processing – Part II”, JMEMS 12, 761-778 (2003).

# Considerations for etching

- Isotropic
  - Etch rate the same in all crystal directions
- Anisotrpoic
  - For wet etches, rate depends on crystal plane
  - For dry etches, directionality determined by process
- Selectivity
  - Etch rate of substrate vs. etch rate of mask
- Mask Adhesion (for wet etching)
  - Increased etching along mask/substrate interface
- Temperature
  - Reaction rate limited?
- Stirring
  - Mass transfer limited?

# Isotropic Etching

- Etch rate is independent of orientation
- Isotropic etch profile
  - Assume a well-adhered mask with infinite selectivity
  - Mask undercut, rounded etch profile



- Applications
  - Flow channels
  - Removal of sacrificial layers in surface micromachining

# Isotropic etching

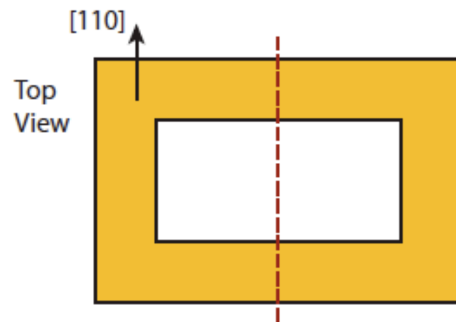
- Some wet etches:
  - Si mixture of nitric, acetic, and HF
  - $SiO_2$ buffered HF (BOE), also HF vapor
  - SiN hot phosphoric acid
  - PolySi KOH
  - Al PAN etch (phosphoric, acetic, nitric acids)
- Some dry etches:
  - Si $XeF_2$ vapor
  - Organics $O_2$ plasma
- Mostly clean enough for front enf, with the exception of KOH, which is a contamination risk for very high T processes. $XeF_2$ vapor is often used as a final release etch

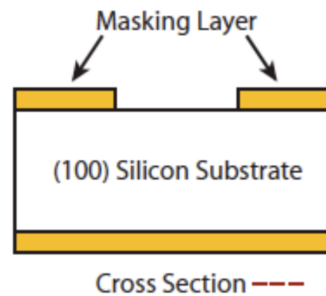
# Anisotrpoic wet etching

- Depends on having a singe-crystal substrate
- The effect depends on the different etch rates of different exposed crystal planes
- Silicon etchants for which <111> planes etch slowly
  - Strong bases (KOH, NaOH, $NH_4OH$)
  - TMAH
  - Ethylene diamine pyrochatechol
  - Hydrazine

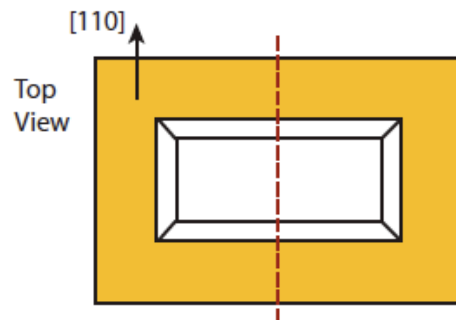
# Making a Trench with KOH

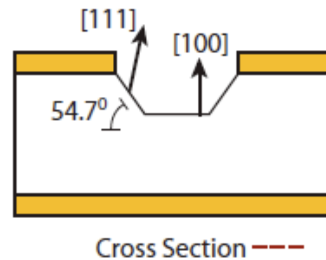
*Before Etching*




*After Etching*

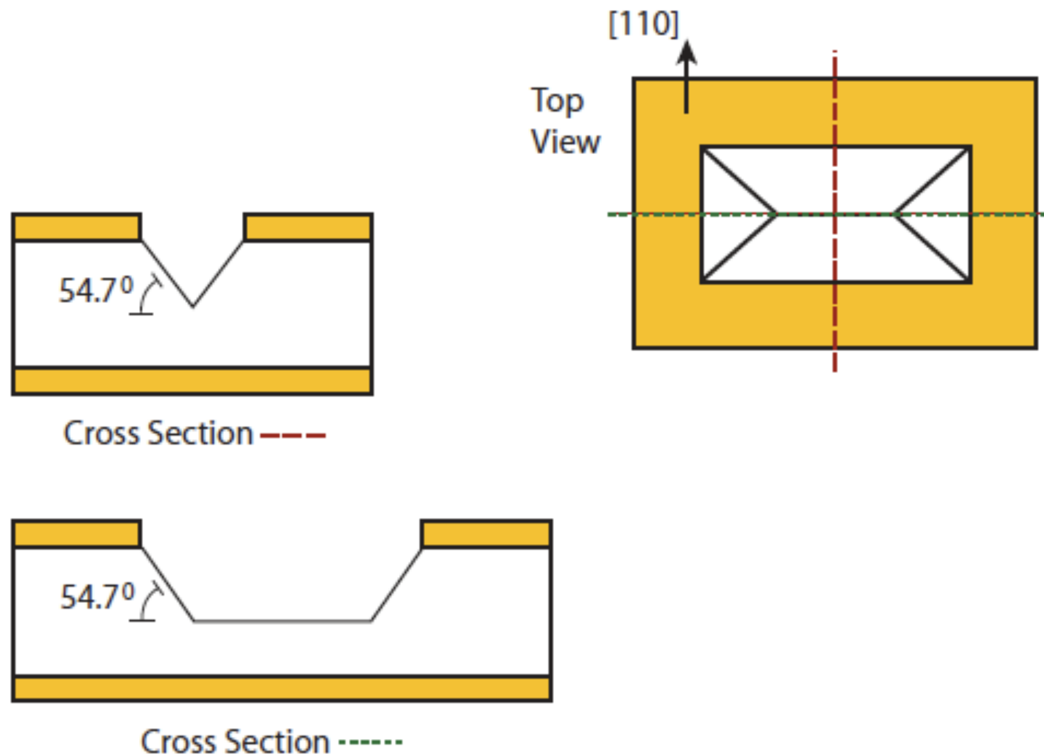



- A rectangular patter is aligned to a [110] direction on a <100> silicon wafer

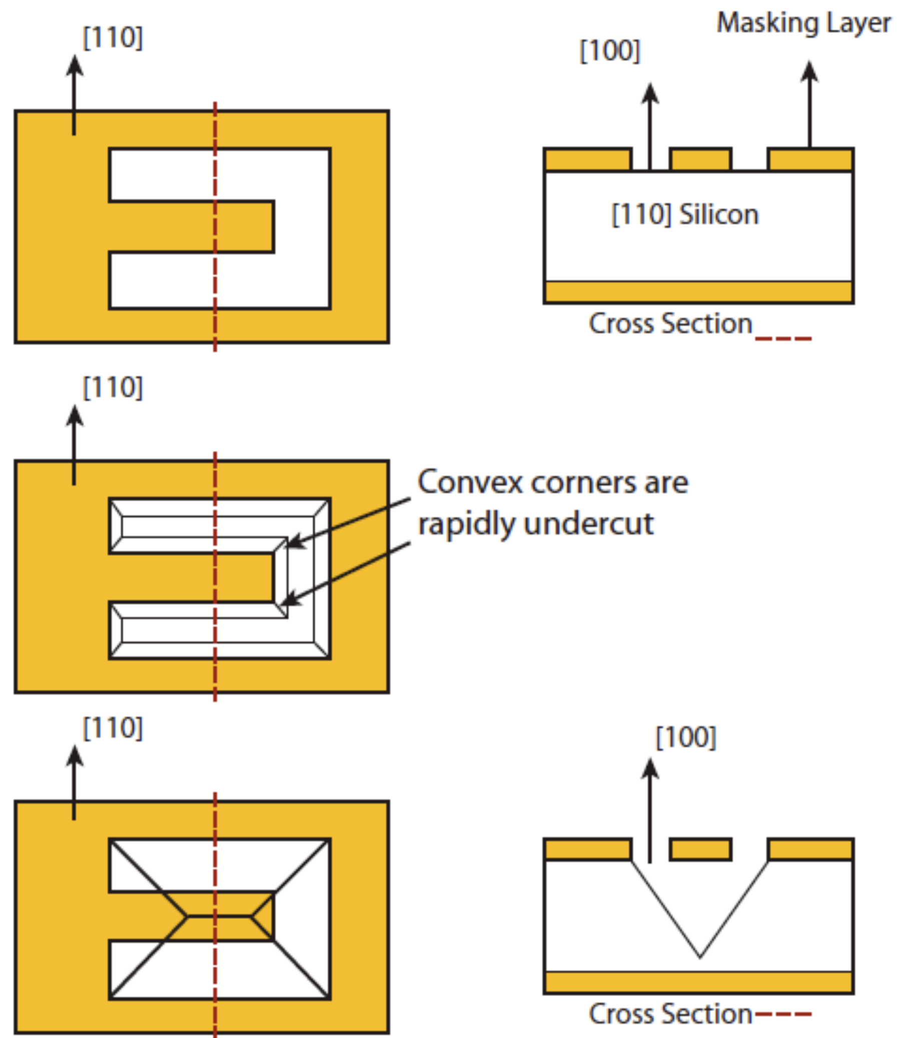
# Making a V-groove

- The previous etch is allowed to go to "termination", i.e. the slowing of etch rate with only {111} planes are exposed (can also make square, pyramidal)

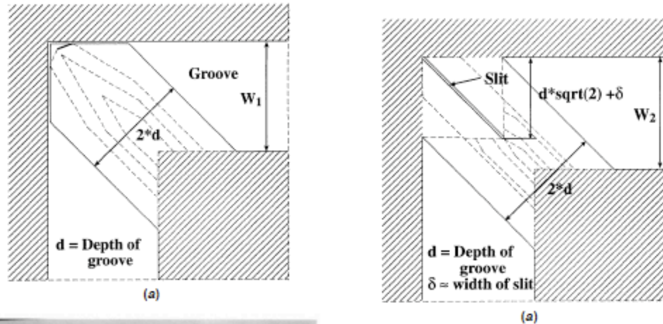


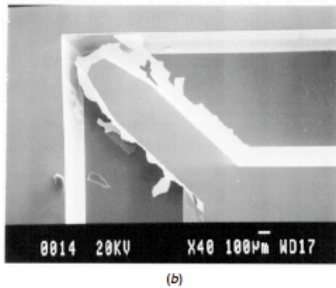
# Convex Corners

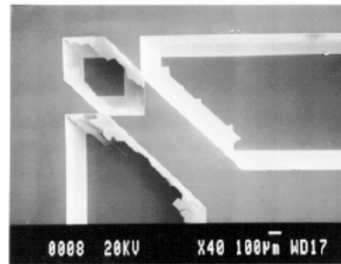
- Convex corners become undercut, as there is no single slow-etching (111) plane to stop on

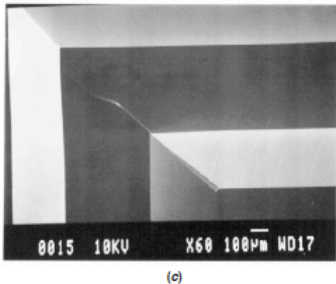


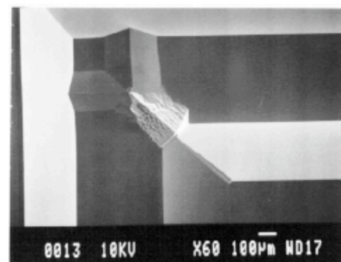
# Corner Compensation



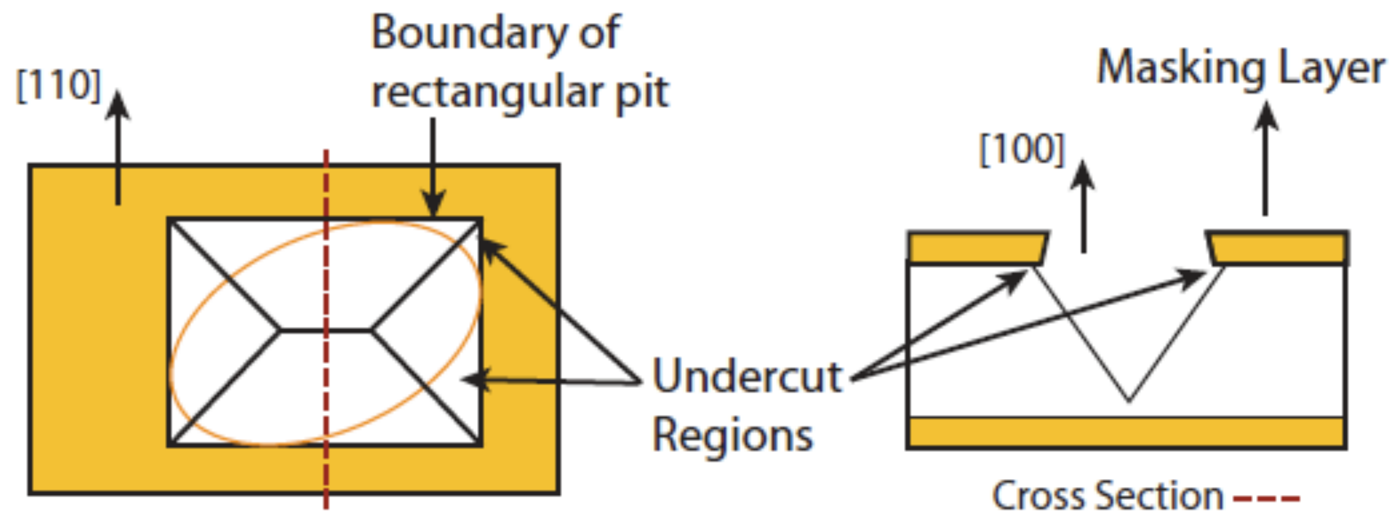




- To etch a convex corner with KOH, add extra material at corner
- Amount of material is chosen so that it will etch away just when the overall etch reaches the desired depth
- Extra material protect convex corner from attack

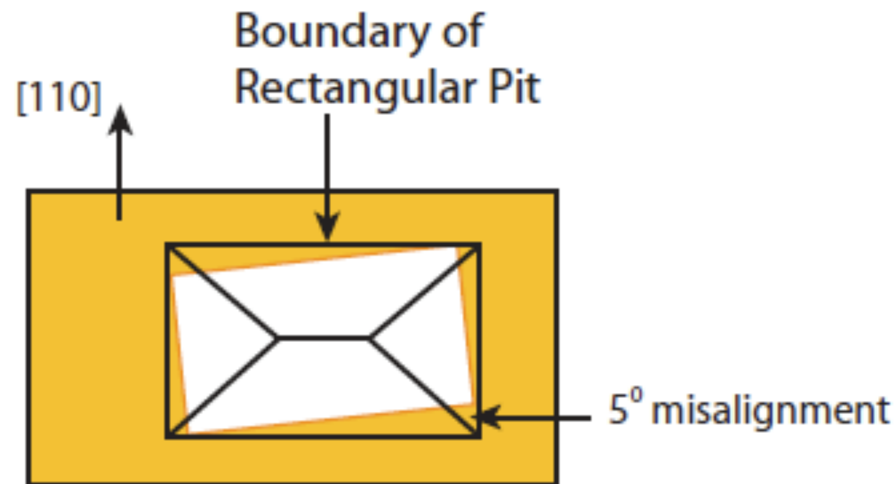
# Arbitrary Shapes

- Any mask feature, if etched long enough, will result in a V-groove tangent to the mask along <110> directions



# Misalignment

- Misalignment of the mask relative to the [110] direction always results in a larger etched region



# Selectivity and etch masks for KOH etches

- Deep etches are long – selectivity matters
- Mask must last long enough to bring the etch to completion
- Sidewall erosion must be at an acceptably slow rate
- Etch rate of {111} planes is finite but small
  - Condition-dependent, of order 400:1 for {100} rate/{111} rate
- Etch rate of mask
  - Si:$SiO_2$ selectivity about 100:1
  - Si:LPCVD SiN selectivity at least 1000:1
  - PECVD SiN not effective (low quality)
  - Do NOT use photoresist!

# Etch Stops

- When etching into a wafer to leave a specific thickness of material, it is necessary to have some kind of etch stop
- Example

# Dry (Plasma) Etching

- At reduced pressure, a glow discharge is set up in a reactive gas environment
- This produces
  - Ions that can be accelerated by the electric fields at the bounding edges of the plasma so that they strike the surface
    - These can be quite directional in their impact
  - Free radicals (uncharged) that can diffuse to the surface and undergo reaction
- Etching depends on reaction followed by creation of a gaseous byproduct which is pumped away

# Applicability

- Most materials can be plasma etched
  - Oxide
  - Nitride
  - Silicon
  - Most Metals (not the noble metals)
  - Polymers
- The art is in achieving suitable selectivity both for masking layers and to layers that ie beneath the layer being etched
  - Known recipes (gas mixtures, plasma conditions) with desired selectivity
  - End-point detection is an important part of “best practice” when using plasma etching

# Shape

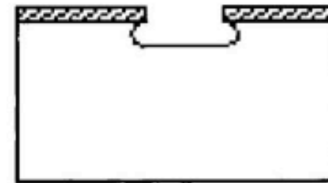
- The higher the pressure, the more isotropic the etch because reactants are scattered many times before reaching the surface (this is called “plasma etching)
- To achieve directional anisotropy, one must go to low pressure to achieve long mean-free paths for the ions (this is called “reactive-ion etching” or RIE)
- Deep reactive ion etching is another thing altogether

# Deep reactive Ion Etching (The Bosch Process)

- Photoresist mask: selectivity about 50:1
- Oxide Mask: selectivity > 100:1
-

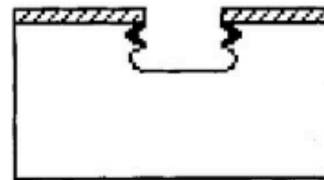
**1. Pattern photoresist**

**2. Reactive ion etch in $SF_6$**



**3. Deposit passivation ($C_4F_8$) (produces a teflon-like polymer)**

**4. Etch and repeat cycle (directional ions clear passivation from bottom only)**



# Depth depends on features and layout

- Features of difference width etch at different rates (recipe dependent)

# Multi-level Etching

- Making multi-level etches can be challenging
- For through etches with two different depths, simply etch from both sides of wafer, with double-sided alignment

**Pattern side 1**

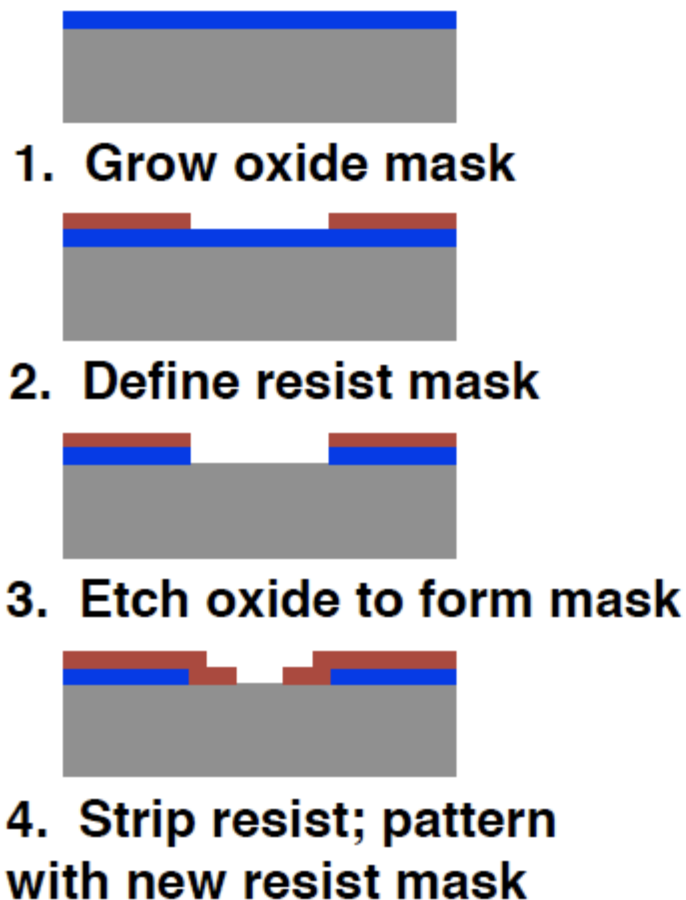
**Etch side 1**

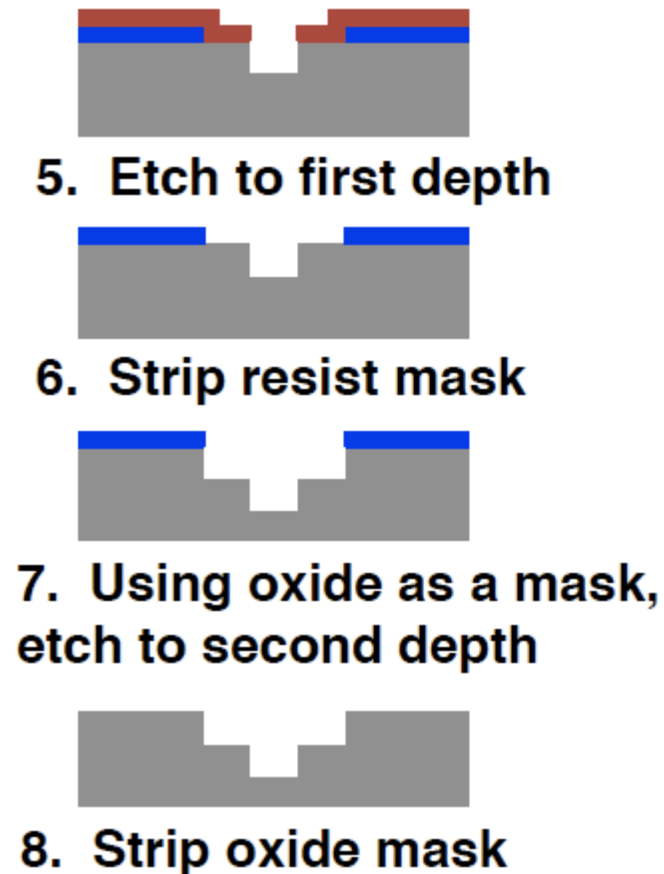
**Flip wafer and pattern side 2**

**Etch side 2**

# Multi-level etching with nested masks

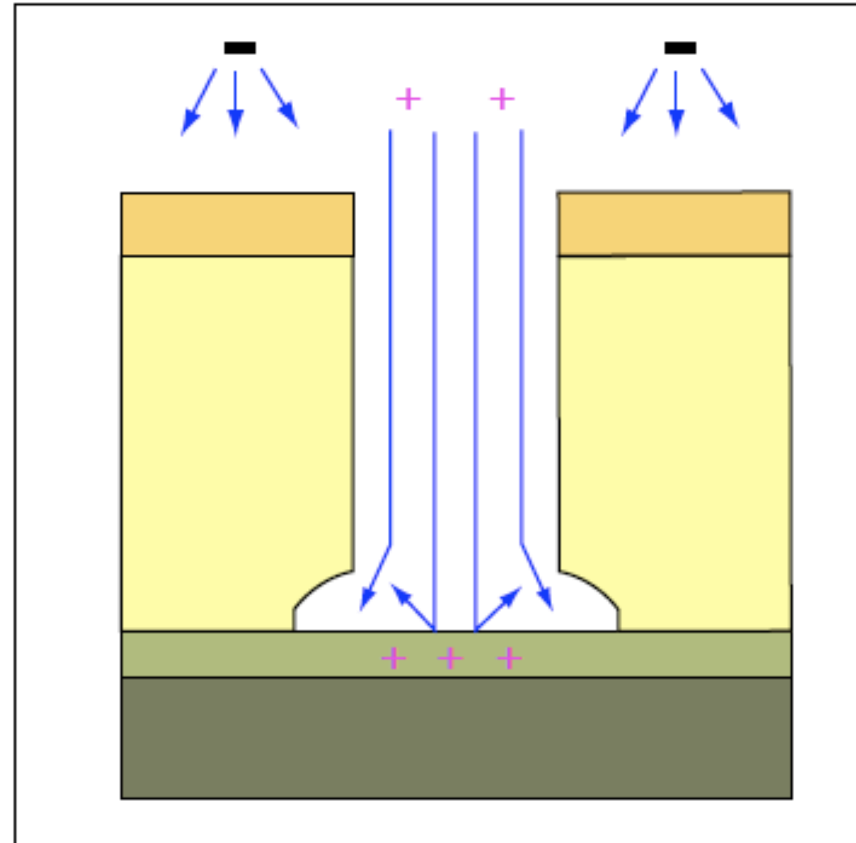
- Etching two sets of deep (> about 10 um) features on the same side of the wafer requires a nested mask



# DRIE with Etch Stop

- SOI substrate
- Buried oxide acts as an etch stop
- Charging can led to “footing”



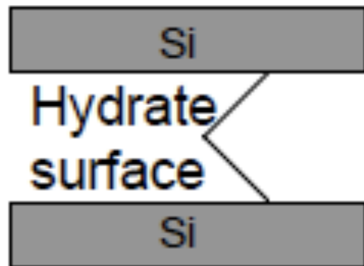
# Microfabrication Outline

- Substrates – Si, SOI, Fused quartz, etc..
- Lithography and patterning
- Doping
- Thin Films
- Etching
- Wafer Bonding
- Surface Micromachining
- Process Integration

# Fundamentals of Wafer Level Bonding

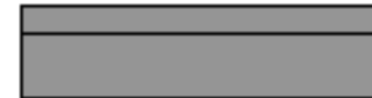
- Two separate and distinct steps
  - The wafers are aligned to each other ina  bond aligner with a possible alignment accuracy of one micron or less
  - The bond fixture is loaded into a vacuum bond chamber where the wafers are contacted together
- There most prevalent types
  - Direct or fusion wafter bonding (high temperature, ~1000C)
  - Anodic or field-assisted bonding (~500C)
  - Bonding with an intermediate “glue” layer
    - Gold (thermocompression), ~300C
    - Polymer or epoxy layer

# Direct Wafer Bonding




Contact and Anneal

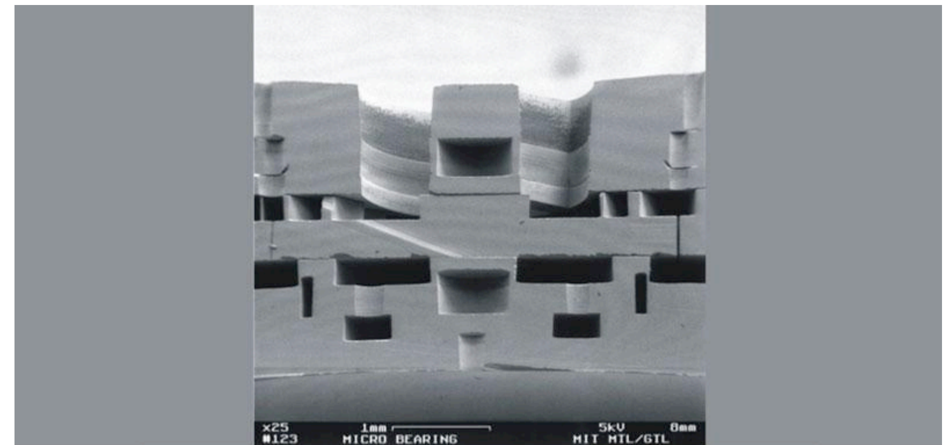
Optional: Thin top wafer



**Spontaneous bonding reduces surface energy; compensates some strain energy cost.**

**Si to Si, Si to oxide, oxide to oxide.**

**A high quality Si to Si bond can have bulk strength.**




8-layer direct bond cross-section.
**Courtesy of MIT.**

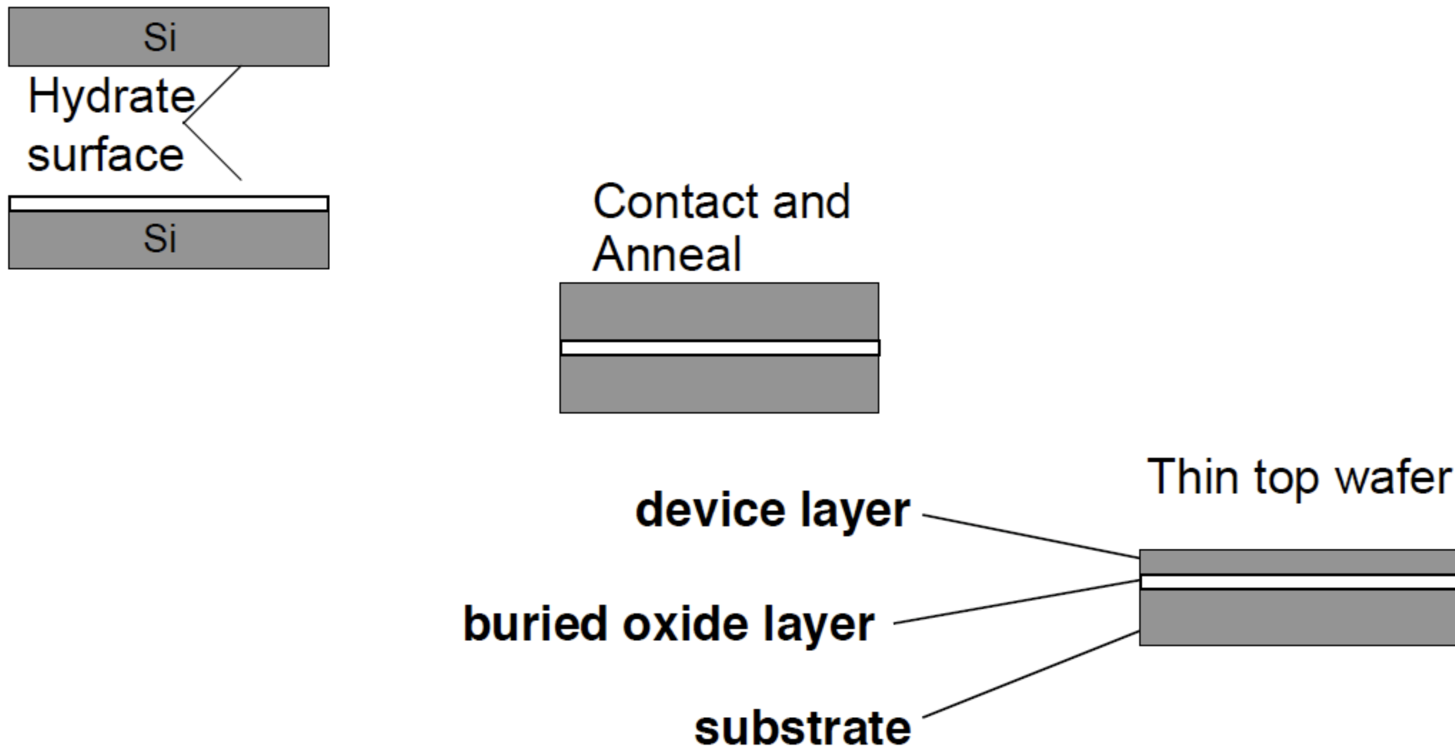
# IR Visualization of bond formation

**Kevin Turner, 2003.**

Courtesy of Kevin Turner. Used with permission.

# Silicon-on-insulator

- Bonding to oxidized wafers is also possible, leading to silicon-on-insulator wafers

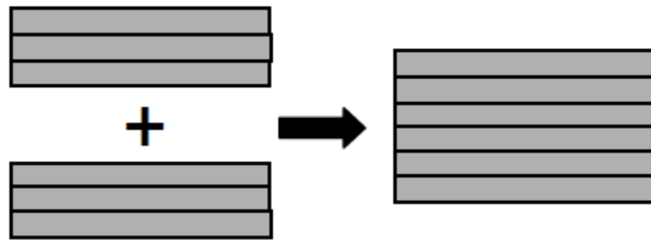


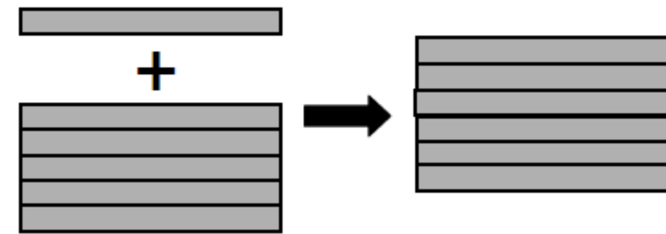
# Wafer geometry impacts bonding

- Spontaneous wafer bonding reduces surface energy
  - Two smooth, clean, perfectly flat wafers will bond spontaneously
- When wafers are not perfectly flat, bonding requires them to bend
  - Strain energy increases
- How far will two wafers bond?
  - Wafers bond until the surface energy reduction equals the strain energy costs
- Important factors
  - Wafer thickness
  - Radius of curvature
    - Wafer bow – innate or from stressed films
    - Waviness – locally greater curvature

# Wafer Geometry Impacts Bonding

- Bonding order and strain energy
  - For given total stack thickness, the strain energy accumulates fastest for wafers of equal thickness (goes as thickness cubed)
  - To bond n wafers, add them one at a time




BAD GOOD

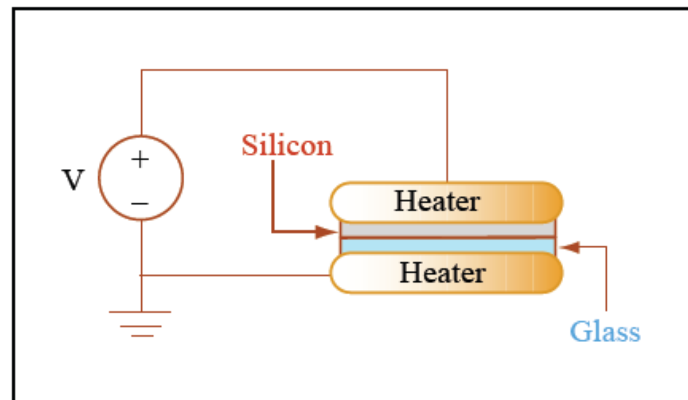
- Etched features
  - Shallow etch hinders bonding (less interaction area)
  - Deep etch aids bonding (less stiffness)

# Wafer bonding and yield

- Yield in MEMS can require a whole-wafer outlook, unlike IC processing
- A micon-scale defect can create a mm- to cm-scale defect
  - Amplification by wafer stiffness
- Can have a die yield of 100% on individual wafers and not get any devices if defects outside the die area prevent wafer bonding
- Cleanliness (particulates, organics) is critical to prevent defects; organics can outgas on anneal
- Adjust process to minimize stiffness in bonding
  - At least one of the wafers should be thin (and therefore relatively pliable) when going into the bonding process

# Anodic Bonding

- The mobility of sodium ions in the glass drives anodic bonding
- The wafers are heated to temperatures of about 500C; a positive voltage (300V – 700V) applied to the Si repels sodium ions from the glass surface
- Suspectible to particulates, but less so than direct bonding
- Commonly used as a packaging step



# Designing process flows for cleanliness

- If you are planning to do a fusion bond, design your process flow to prevent exposure of boding surfaces to junk
    - ➢ Cleanliness is a good idea for anodic bonding, too, but anodic bonding is less pricky
- Some junk washes off easily, but some doesn’t
- Example: deep reactive ion etching’s passivation layer is reluctant to come off (ashing helps somewhat but isn’t perfect)
- Work around: if possible, start your process by coating your wafer with a protective layer, like oxide. When you remove it right before bonding, it carries the junk away from it

# Microfabrication Outline

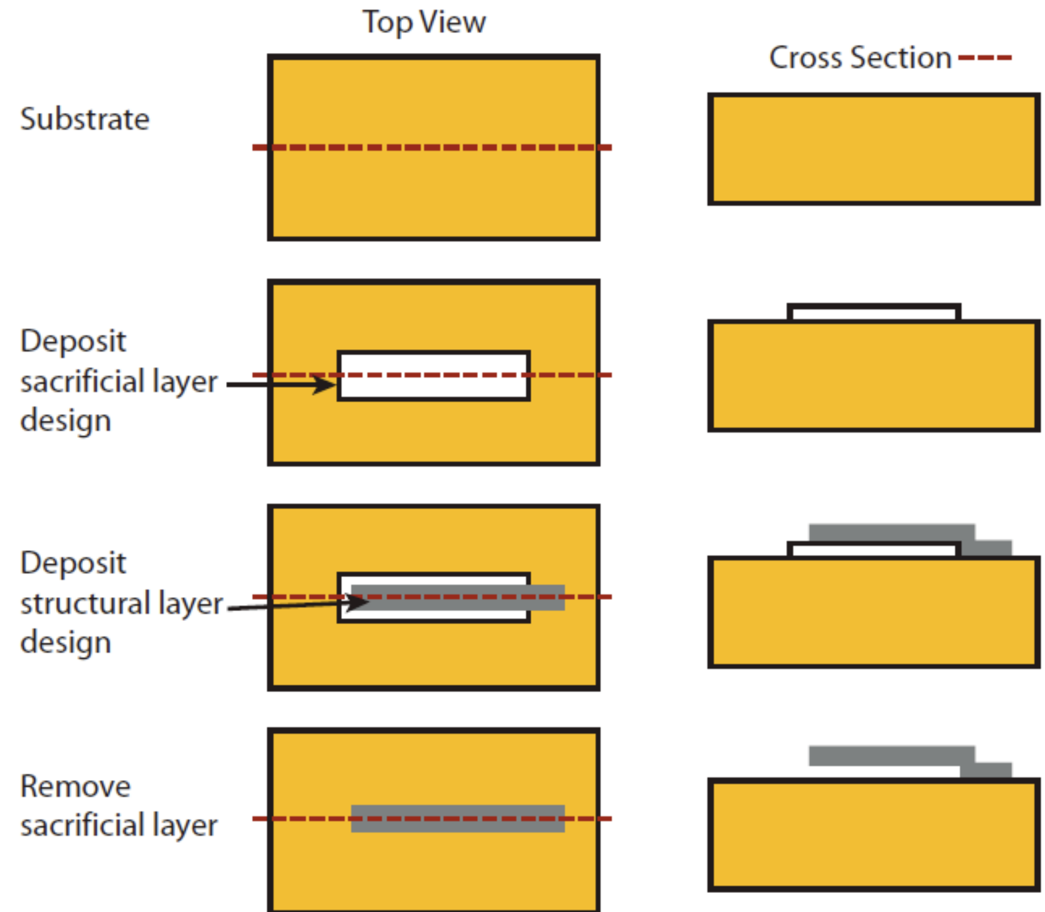
- Substrates – Si, SOI, Fused quartz, etc..
- Lithography and patterning
- Doping
- Thin Films
- Etching
- Wafer Bonding
- Surface Micromachining
- Process Integration

# Surface Micromachining

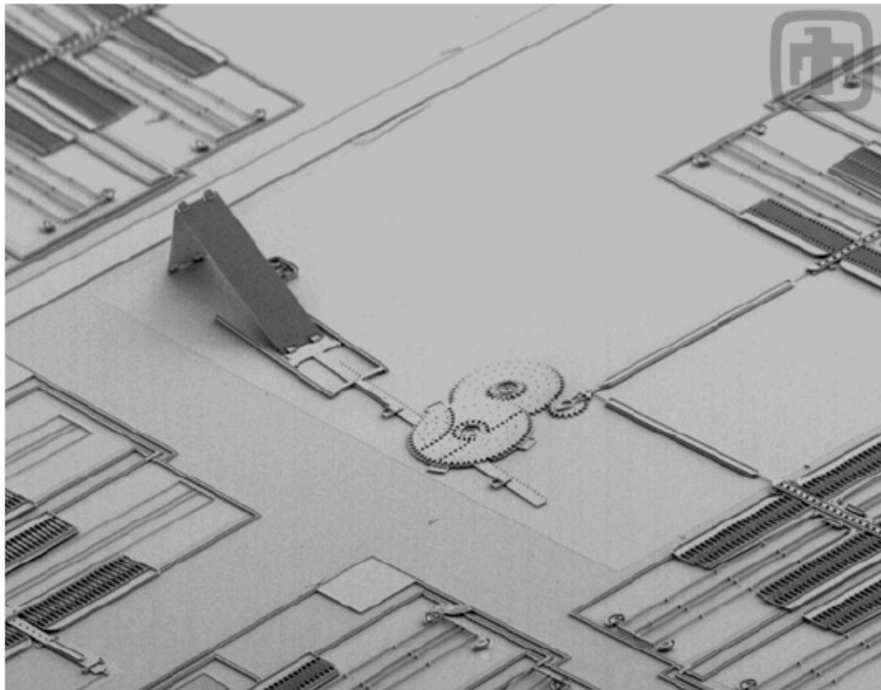
- Surface micromachining refers to the selective removal or sacrificial layers beneath structural layers to create suspended structures
- Many materials choices possible
- Structural polysilicon and sacrificial PSG oxide is well developed, fully characterized, and available as a foundry service
- Why use surface micromachining?
  - Complex multi-layer structures are possible without the need for wafer bonding
  - Structure thickness is controlled by thickness of deposited film, not by etch

# Illustrating surface micromachining

- Example
  - Structural layer:
    - Polysilicon
  - Sacrifical layer:
    - Oxide
  - Etchant
    - HF



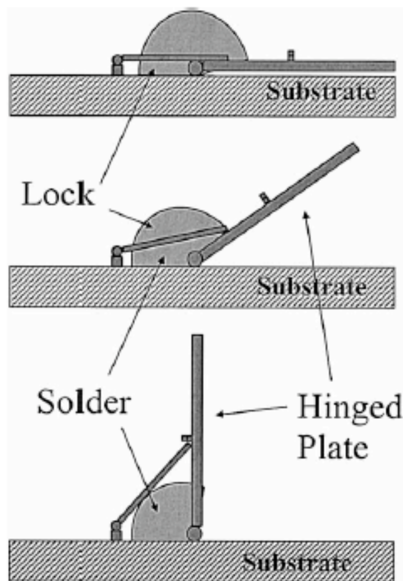
# Surface Micromachining

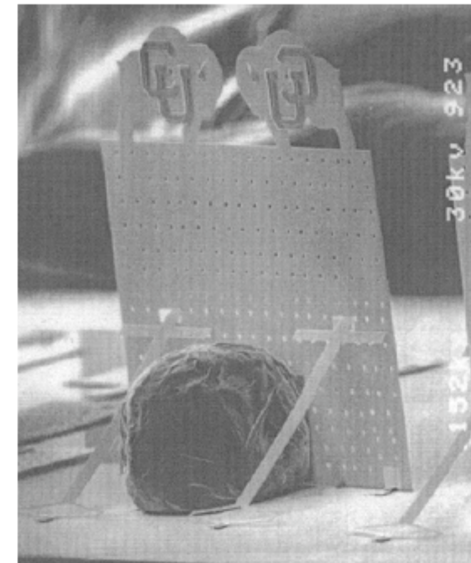


- In-plane processing; potentially out of plane structures

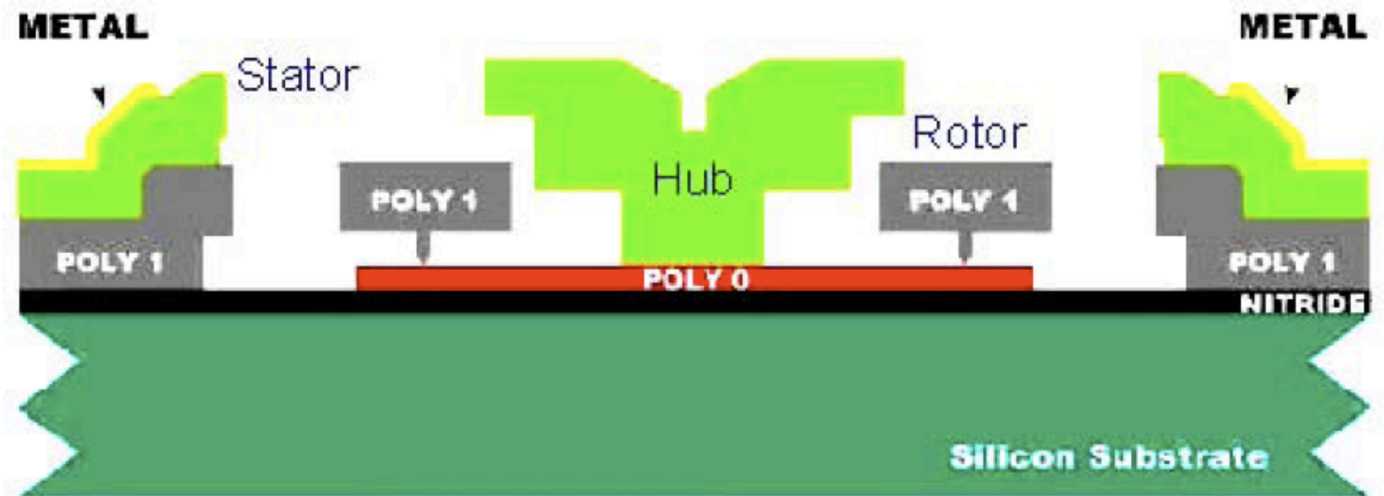
# Solder assembly of surface micromachined parts

- Build surface micromachined parts
- Place solder over joint
- Melt sode;r surface tension bends part up until it hits limited



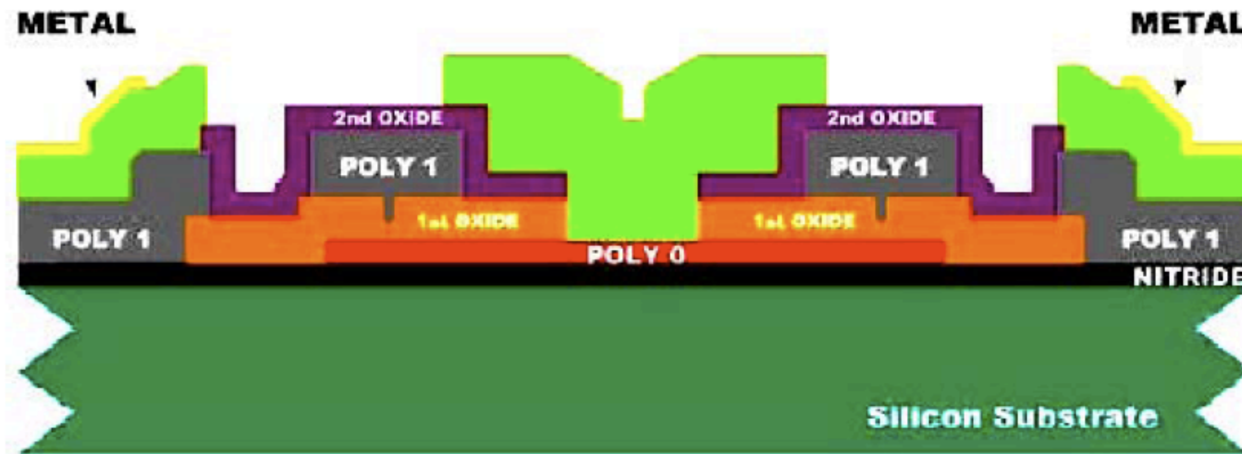
# Introduction to MUMPs




Courtesy of MEMSCAP, Inc. Used with permission.

**PolyMUMPs (Multi-User MEMS Process) is a three-layer polysilicon surface micromachining commercial process established in BSAC and now available from MEMSCAP.**

# MUMPs Process




Courtesy of MEMSCAP, Inc. Used with permission.

**Cross section before sacrificial etch**

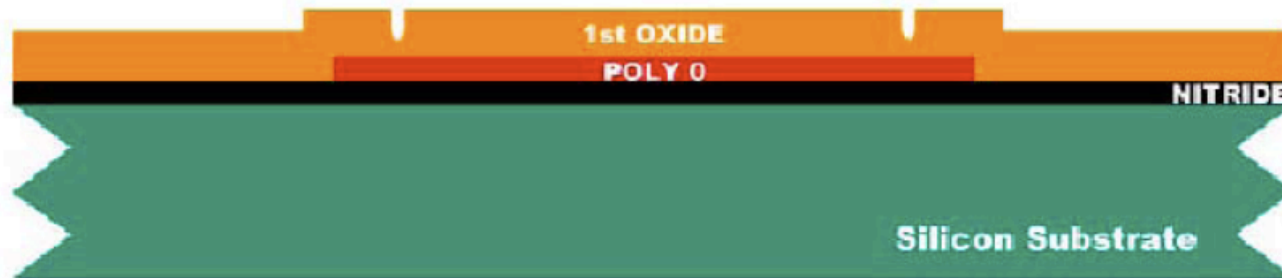
- ❑ **Structural layers: Poly 0, Poly 1, Poly 2**
- ❑ **Sacrificial layers: Oxide 1, Oxide 2 (phosphosilicate glass)**
- ❑ **LPCVD nitride acts as passivation, electrical isolation layer**

# MUMPs Process: Step 1

Courtesy of MEMSCAP, Inc. Used with permission.

- ❑ **4” 100 silicon wafers, 1-2 Ω resistivity**
- ❑ **600 nm LPCVD $Si_3N_4$**
- ❑ **500 nm LPCVD polysilicon (Poly-0)**
- ❑ **Lithography poly-0 (Hole 0) and RIE poly-0**

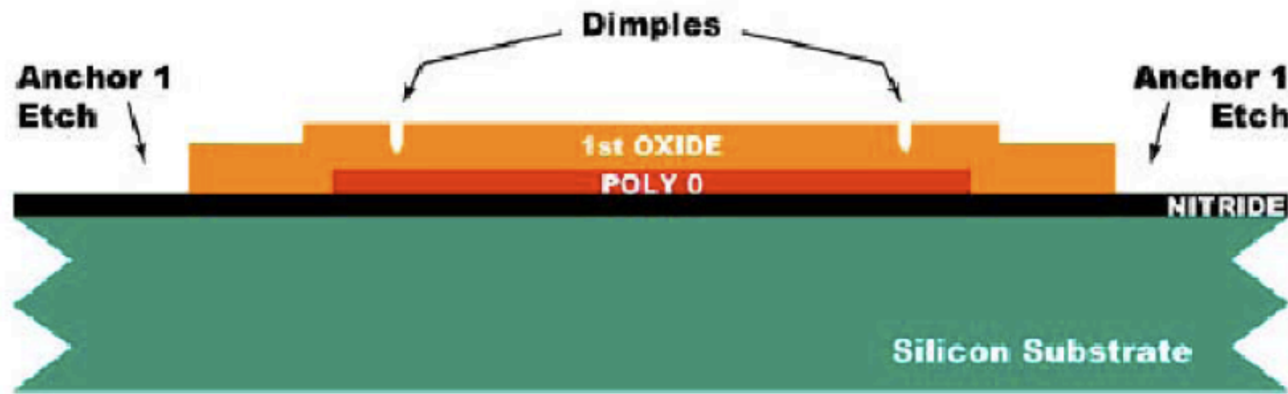
# MUMPs Process: Step 2




Courtesy of MEMSCAP, Inc. Used with permission.

- ❑ **2.0 μm LPCVD PSG (oxide-1) and 1050 °C anneal**
- ❑ **Lithography Dimples and RIE PSG (750 nm)**

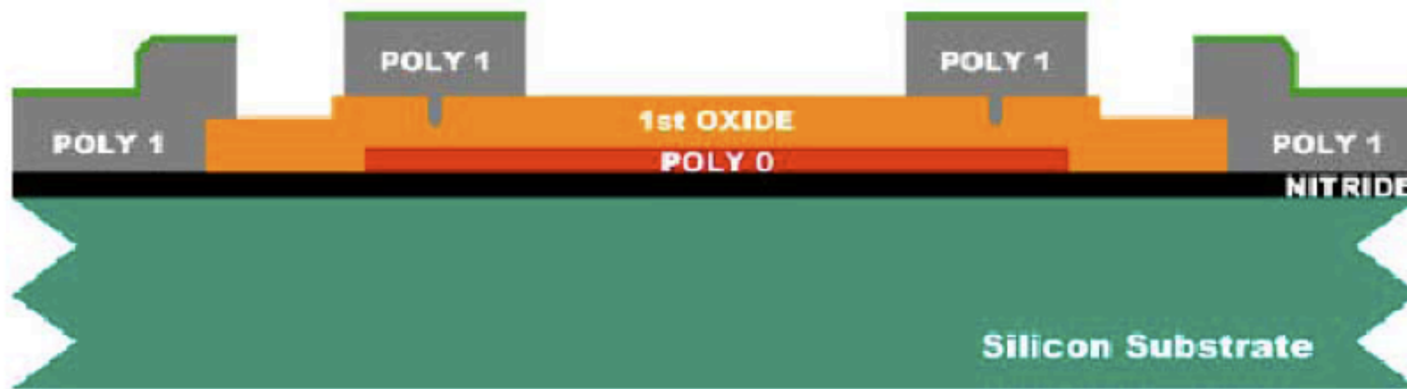
# MUMPs Process: Step 3




Courtesy of MEMSCAP, Inc. Used with permission.

- **Lithography Anchor1 and RIE PSG**

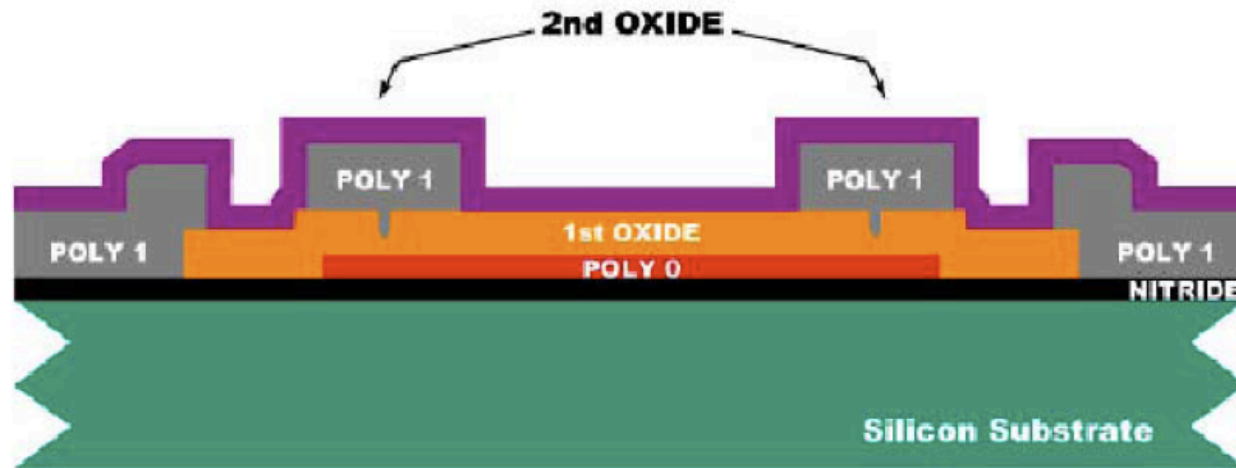
# MUMPs Process: Step 4




Courtesy of MEMSCAP, Inc. Used with permission.

- **2.0 µm LPCVD polysilicon (poly-1)**
- **Lithography Poly-1 (Hole 1) and RIE poly-1**

# MUMPs Process: Step 5




Courtesy of MEMSCAP, Inc. Used with permission.

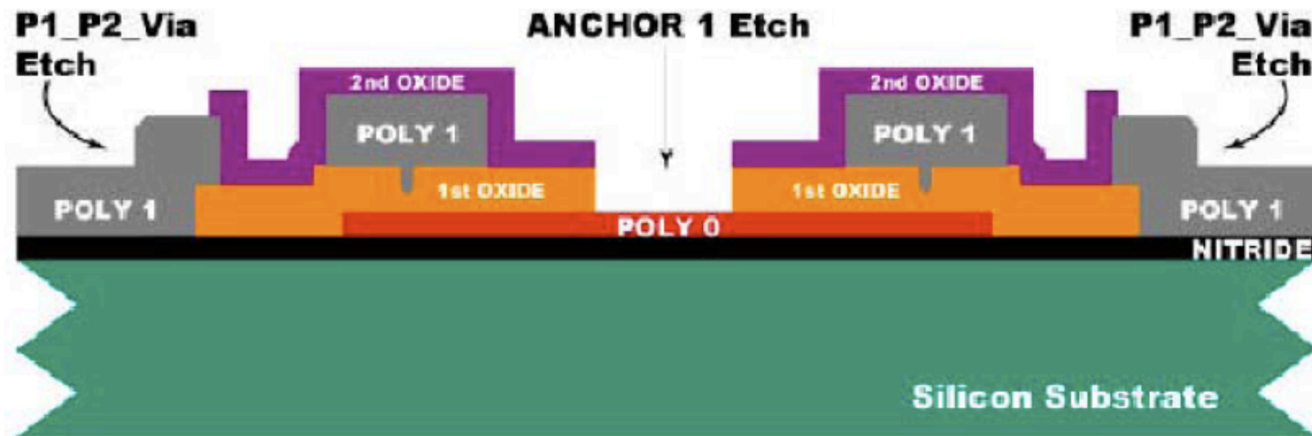
- ❑ **0.75 μm LPCVD PSG(oxide –2 ) and 1050 °C anneal**

# MUMPs Process: Step 6

Courtesy of MEMSCAP, Inc. Used with permission.

- Lithography poly 2-poly1-via and RIE PSG (oxide 2)

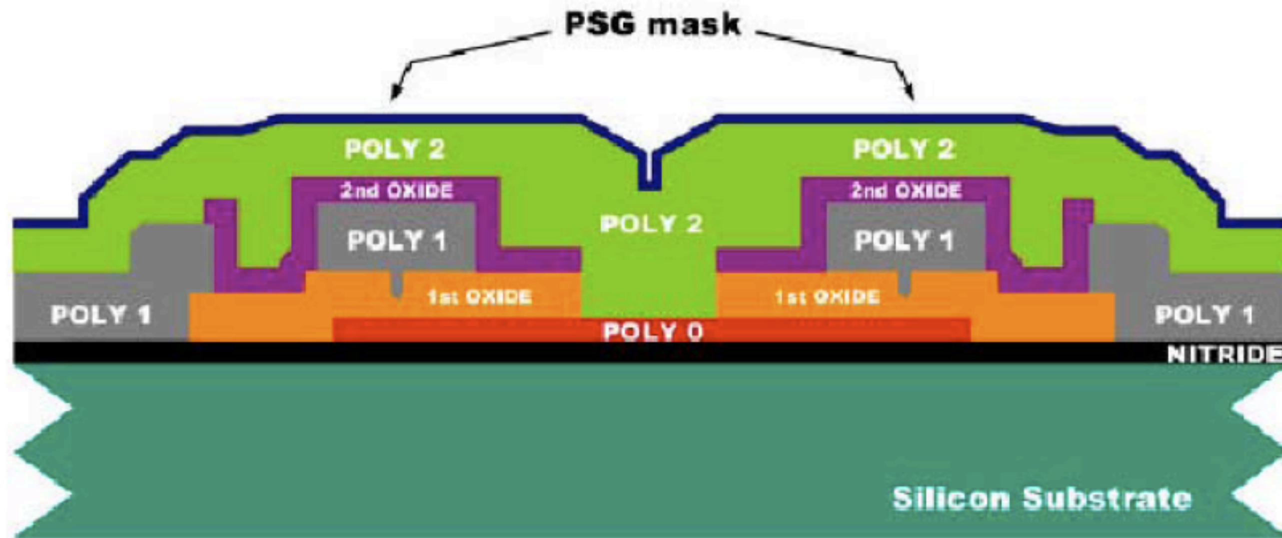
# MUMPs Process: Step 7




Courtesy of MEMSCAP, Inc. Used with permission.

- **Lithography Anchor 2 and RIE PSG (oxide-2 and oxide-1)**

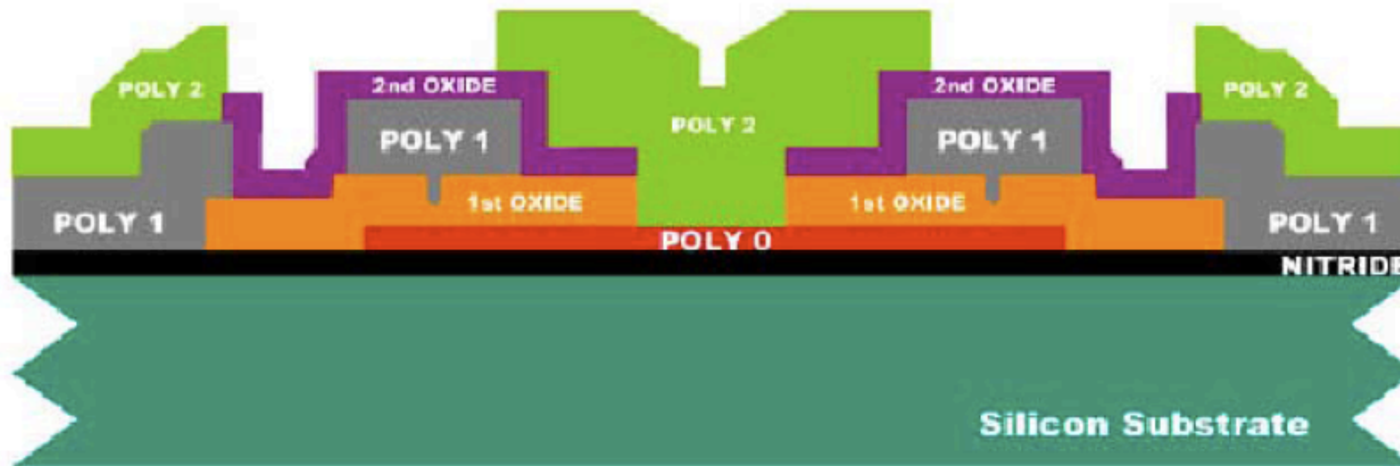
# MUMPs Process: Step 8




Courtesy of MEMSCAP, Inc. Used with permission.

- ❑ 1.5 μm LPCVD polysilicon (poly-2)

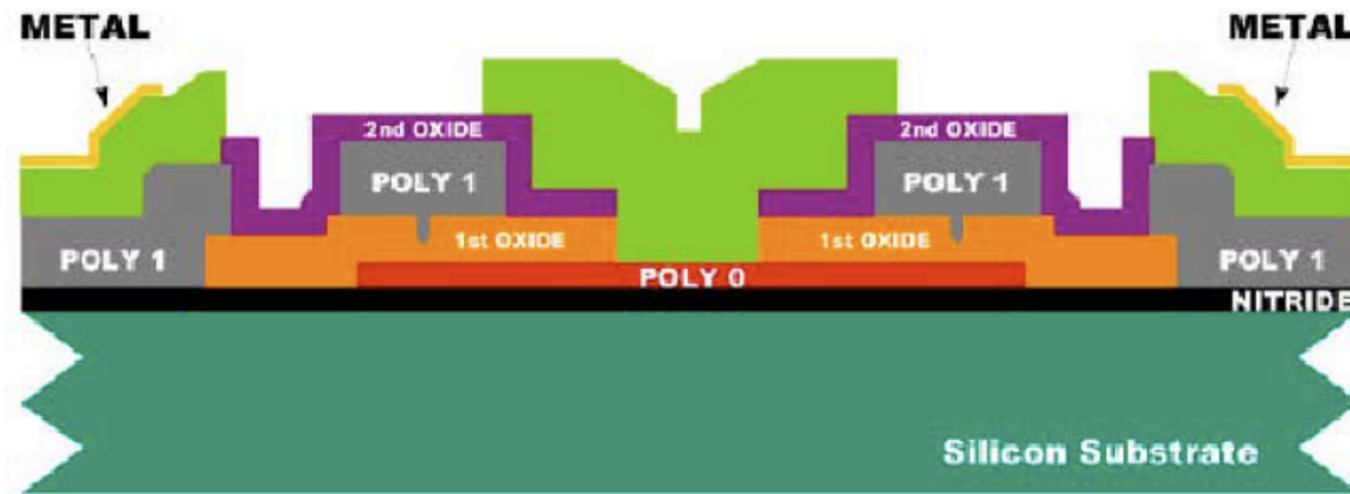
# MUMPs Process: Step 9




Courtesy of MEMSCAP, Inc. Used with permission.

- ❑ **Lithography poly-2 (Hole 2) and RIE poly-2**

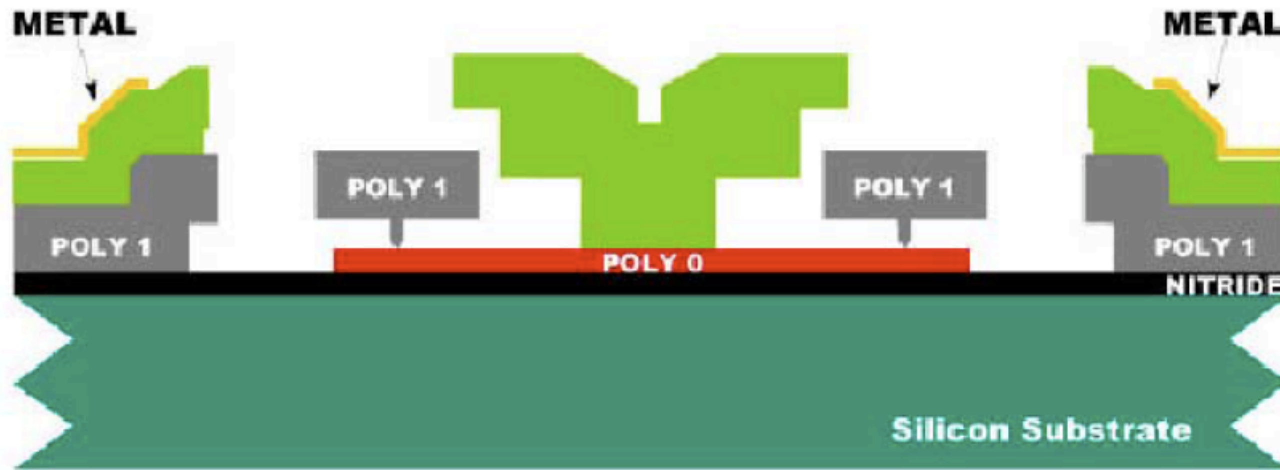
# MUMPs Process: Step 10




Courtesy of MEMSCAP, Inc. Used with permission.

- **0.5 μm Cr/Au evaporation (Metal)**
- **Lithography Metal (HoleM) and lift off**

# MUMPs Process: Step 11




Courtesy of MEMSCAP, Inc. Used with permission.

**Releasing**

- ❑ 1.5-2 min 49% HF sacrificial oxide etch at room temp.
- ❑ $CO_2$ critical point drying

# Stiction

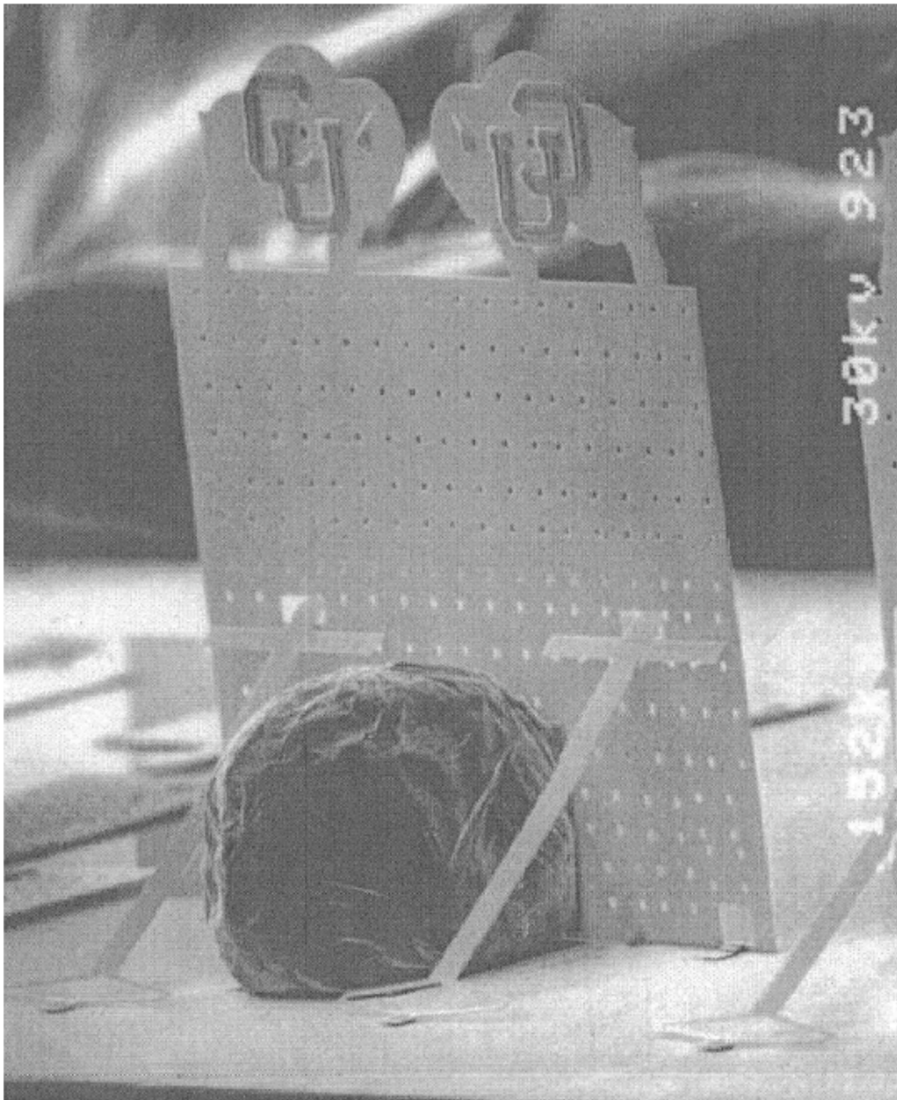
- Permanent adhesion between movable structures or structure and substrate
- Caused mainly by van der waals forces due to hydrogen content of moisture on surface and close proximity of movable structures (due to thin films used)

- Dealing with stiction:
  - Thin structures are susceptible
    - Deposited films
    - Narrow, deep-etched structures
  - Prevention is key
  - Options:
    - Low surface tension liquid rinse after sacrificial etch
    - Surface roughening or hydrophobic surface coating
    - Critical point $CO_2$ of sublimination drying to prevent meniscus formation

# One release recipe

- **Acetone soak to remove photoresist (30 min)**
- **Isopropanol soak to remove acetone (30 sec)**
- **Rinse in water to remove isopropanol (1 min)**
- **Soak in 49% HF (3:30 min)**
- **Soak in 4:1 methanol/water (9 min)**
- **$CO_2$ supercritical release. Liquid $CO_2$ is used to flush the methanol. The $CO_2$ is then heated and will subliminate around 35 °C.**

# HF only removes the oxide that it can reach




- Holes in plates are important!

# Microfabrication Outline

- Substrates – Si, SOI, Fused quartz, etc..
- Lithography and patterning
- Doping
- Thin Films
- Etching
- Wafer Bonding
- Surface Micromachining
- Process Integration

# Concerns in designing a process ad mask set

- We know that we have to obey the laws of physics and the vendor's constraints when designing a process flow
- Its easier to design a robust, effective process if you've designed your device well
  - Selecting your device architecture wisely – if you don't design an unbuildable structure, you won't have to built it
  - Designing the package and packaging process during the device design
    - How are you going to interface this device to the real world?

# One concern: accumulated topography

- Successive steps of lithography and etching or deposition create non-planar surface topography
- This can interfere with further fabrication:
  - Getting good coverage with photoresist
  - Depth of focus of lithographic tool
  - Wafer bonding
  - Stringers left over from etching
- Chemical mechanical polishing (CMP) can be used to remove or reduce unwanted topographic features
- Other techniques available for special cases

# Chemical Mechanical Polishing (CMP)

- Often used to planarize interlayer dielectric insulators
- Typical surface roughness less than 1 nm, but waviness can be much bigger
- Combination of mechanical polishing and chemical etching
- Using an abrasive slurry dispersed in an alkaline solution
- High, narrow features polish faster than low, uniform features

# Stringers

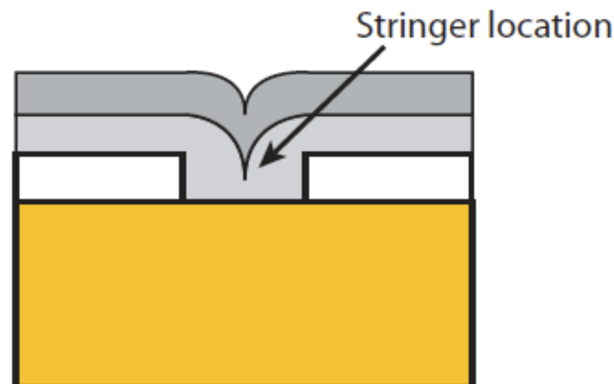
- Stringers form when a conformal film that covers topographic features is etched directionally, e.g. with RIE or dilute plasma

Conformal coating over steps

Stringers remain after directional plasma etch.

# A Bad Stringer Location

- The material in the cusp is almost impossible to remove by etching
- Using a thicker white layer and polishing it back with CMP cures the stringer problem (so part of the cure is “don’t let it happen in the first place”…a good lesson to remember)



# System partitioning

- You know that the overall system requires a set of functionalities. How many of them should you put on the MEMS chip? This will govern your fab process!
- Prime example: electronics
  - If you have a tiny signal that you can't detect without amplifying it as soon as it's produced, then you need at least first stage amplifying electronics
  - If on-chip electronics are not functionally required, you must choose whether it will save you money (fewer chips to make and package together) or cost you money (more ways to ruin your MEMS chip in the fab, and fewer process options) to include electronics on chip

# Die Separation

- Usually, you use single MEMS chips, rather than whole wafers
- When and how to cut the chips apart?
- If you're going to slice them apart with a (very ungentle) die saw, you must identify where in the process you will do it without breaking your structures
- One alternate approach: include etch features on your mask that will separate the dies most of the way so they snap apart at the end
- Either way, must think about this when creating your process flow

# Design MEMS device and packaging together!

- You can’t make the microfabricated part without photomasks
- The photomasks include interfaces to package:
  - Electrical bond pads, access required for MEMS function
- Until you make the system partitioning decision, you don’t know the bond-pad requirements
- Until you design the package, you don’t know what the constraints on the physical access will be
- Therefore, until you make the system partitioning decision and design the package, you can’t make the masks!
- Second order package-device interactions:
  - High temperature packaging step can affect device: thermal stresses, outgassing, etc…

# Process design philosophy

- People publish their fab accomplishments
- Students read the papers and take home the wrong message
  - “They published X. X must be straightforward, and my process can probably count on accomplishing even a little more X”
  - “W,X,Y, and Z have all been demonstrated. I can’t count on doing any better than W, X, Y, and Z, but I’m sure I can accomplish them simultaneously”
- Some advice:
  - Don’t’ design your processes on the hairy edge of impossibility
  - Including a very difficult process may be unavoidable, but a) don’t include a lot of them and b) be prepared to put a lot of work into making a process robust

UCSB
nanolab

THE UNIVERSITY OF CALIFORNIA
1868

UCSB
nanolab

UCSB
nanolab

UCSB
nanolab