ME 141B: The MEMS Class
Introduction to MEMS and MEMS Design

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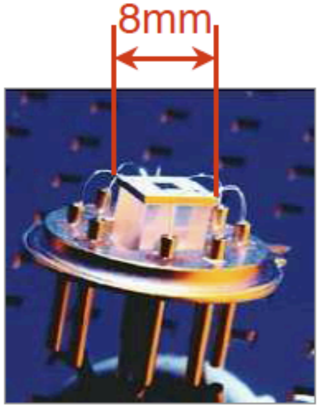
Fundamentals of Wafer Level Bonding

- Two separate and distinct steps
  - The wafers are aligned to each other ina bond aligner with a possible alignment accuracy of one micron or less
  - The bond fixture is loaded into a vacuum bond chamber where the wafers are contacted together
- There most prevalent types
  - Direct or fusion wafter bonding (high temperature, ~1000C)
  - Anodic or field-assisted bonding (~500C)
  - Bonding with an intermediate “glue” layer
    - Gold (thermocompression), ~300C
    - Polymer or epoxy layer

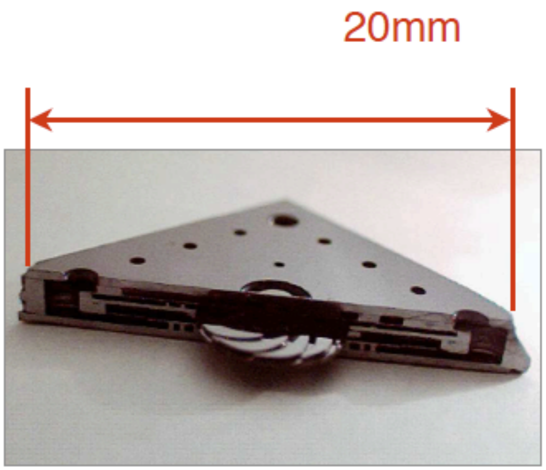
Wafer Bonding Motivation

- For pressure sensors – allows creation of cavities
- For fluidic channels, allows for easy fabrication
- For MEMS device, allows for formation of 3D structures, cavities by combining etched wafers
    - Lithography and etching intrinsically allows limited range of shapes in 3D (prisms, cylinders, “extrusions”)
- For MEMS and microelectronics allows for wafer level packaging
    - Minimize connections from chip to macroscale
    - Hermetic sealing prior to die sawing
    - Parallel manufacturing
    - 3D interconnects

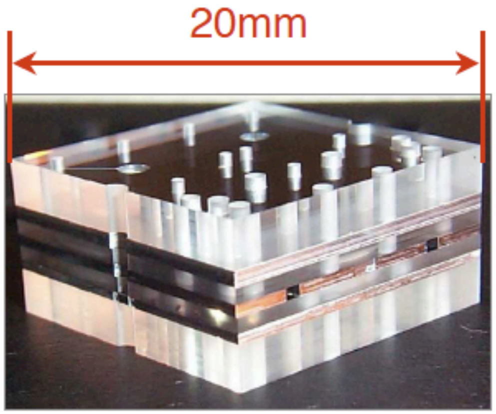
MEMS applications of bonding



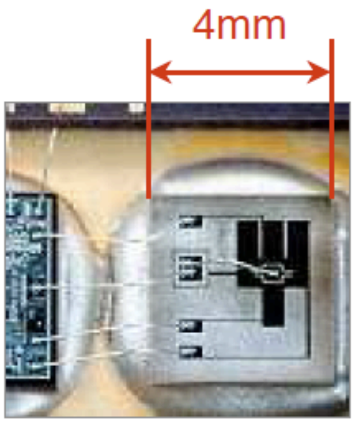
pressure
sensors



microengines



microfluidic
devices



accelerometers

Wafer Bonding Technologies

- Direct Fusion bonding
  - Si to Si (also Si/SiO_2, Si/Al_2O_3)
- Anodic bonding
  - Si to glasses containing conductors
- Glass frit bonding
  - Glass powder/paste softened/sintered to form bond
- Solder/braze bonding (not generally used at wafer level)
- Thermo-compression bonding
- Polymeric adhesives (not generally used for permanent bonding but sometimes used for temporary attachment for handling)

Silicon Direct Bonding

- Grew our of efforts to replace deposition processes for creating device layers or microelectronics (c 1985)
  - Layer transfer by bonding and thinning doped wafer
  - Silicon on insulator (SOI)
- Very rapidly adopted or MEMS
  - Cavity formation
- Commerical application for SOI has driven transition to volume production – mainstream VLSI
  - Process very reproducible, well-controlled
- Evolution to other applications, dissimilar materials

Basics of direct bonding

- Silicon fusion bonding is the process of bonding two mirror-polished silicon wafers with no intermediate adhesive layer
- The baseline process consists of:

Surface preparation → **Align and contact** → **Inspect using IR** → **Anneal**

- The primary advantages include:
  - Bonds with strengths that approach that of bulk silicon
  - No CTE mismatch
  - Compatible with CMOS processing
  - Ability to inspect and re-bond after contacting stage

Cavity formation using Bonding

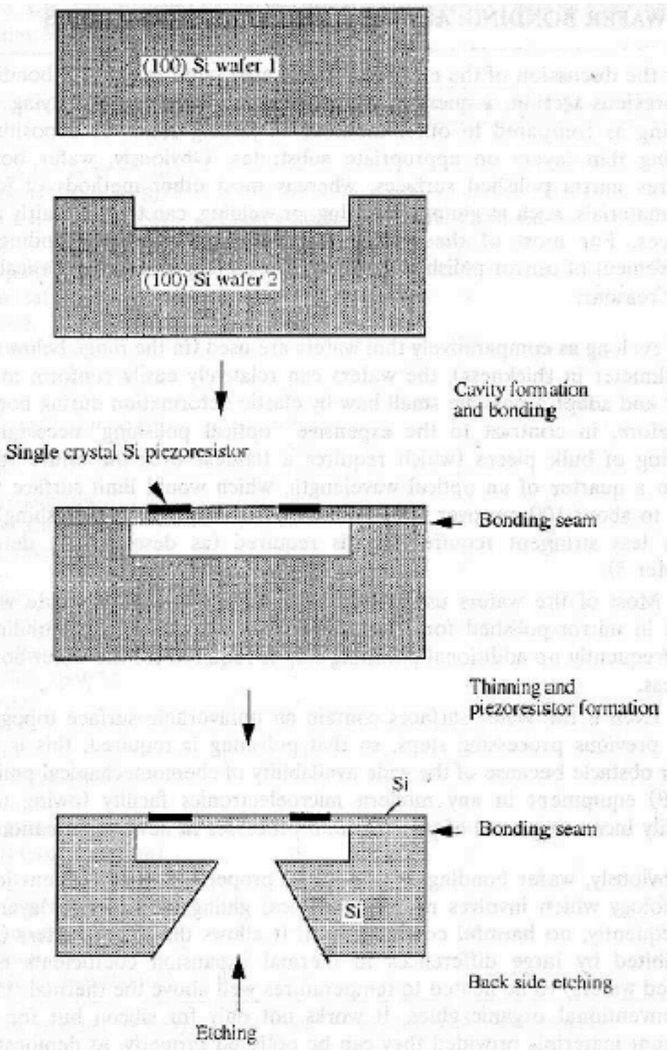
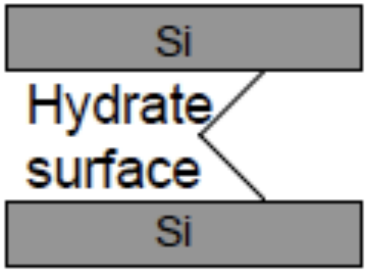
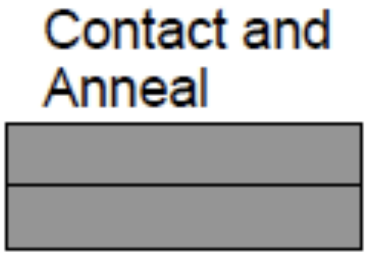
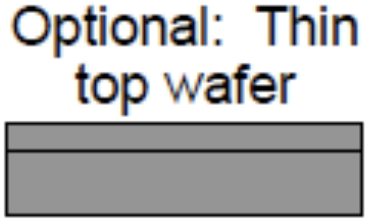


Fig. 1.5 Schematic of pressure sensor fabricated by wafer bonding.

Direct Wafer Bonding



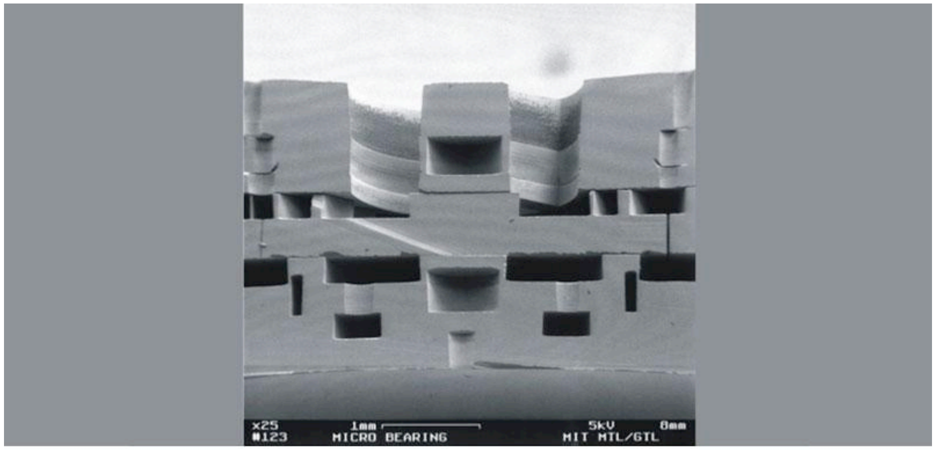




Spontaneous bonding reduces surface energy; compensates some strain energy cost.

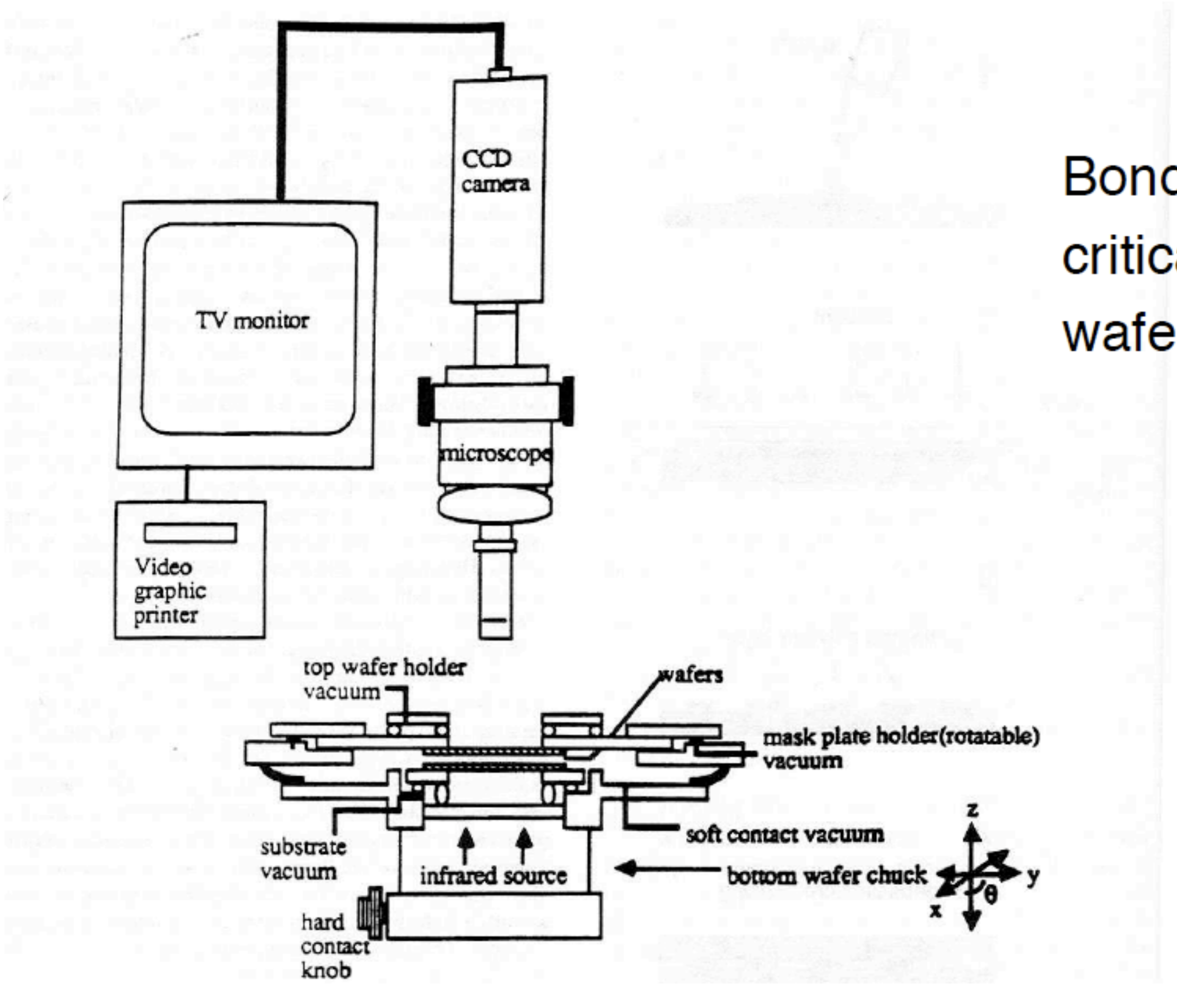
Si to Si, Si to oxide, oxide to oxide.

A high quality Si to Si bond can have bulk strength.



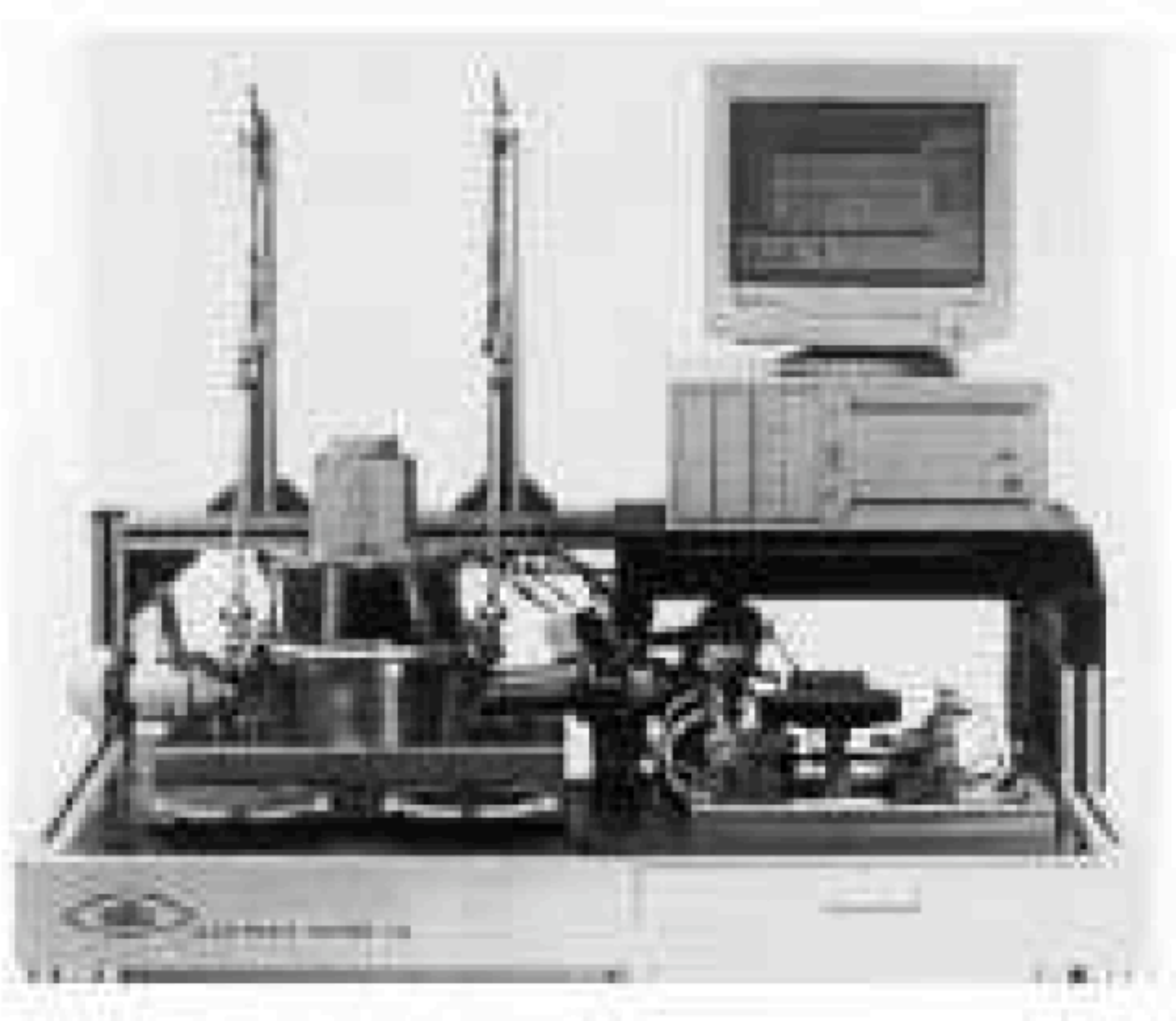
8-layer direct bond cross-section.
Courtesy of MIT.

Alignment fixture for bonding



Bond alignment critical if features on wafers

EV Wafer Bonder



Imaging of Bonds

- Silicon is translucent in infra red at wavelengths of 1 um
- Unbonded regions in close proximity generate interference fringes
- Very useful tool for inspecting bonds after contacting
  - Quick, simple
- Bonds can be separated at this stage, re-cleaned, and re-bonded
- Also can use ultrasound inspection methods
  - Unbonded interfaced generate echos
  - Commonly use in packaging inspections
  - Use for non IR transparent materials

IR Imaging

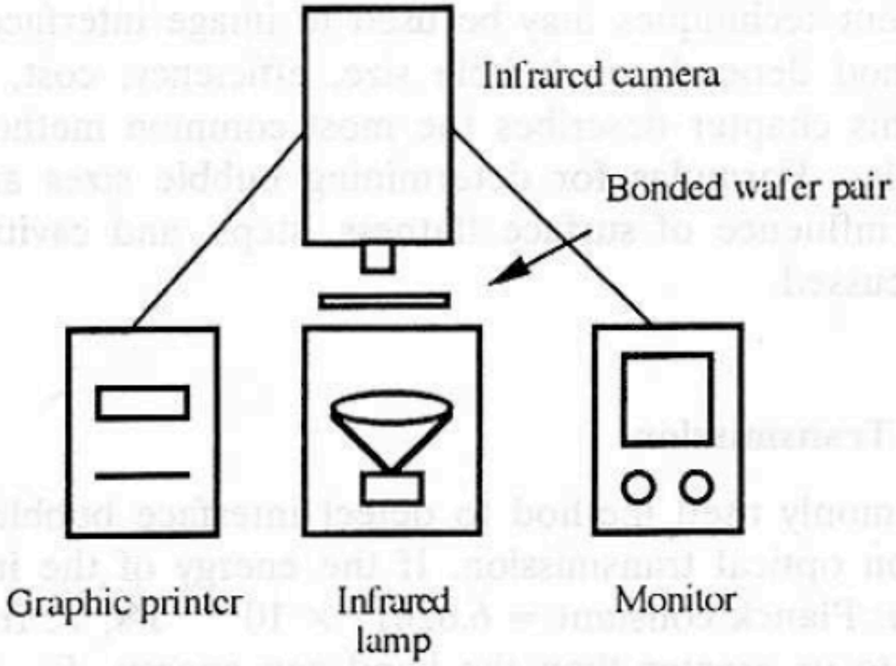


Fig. 3.1 Typical configuration of an imaging system for detecting interface bubbles in bonded Si/Si pairs.

Acoustic Microscopy

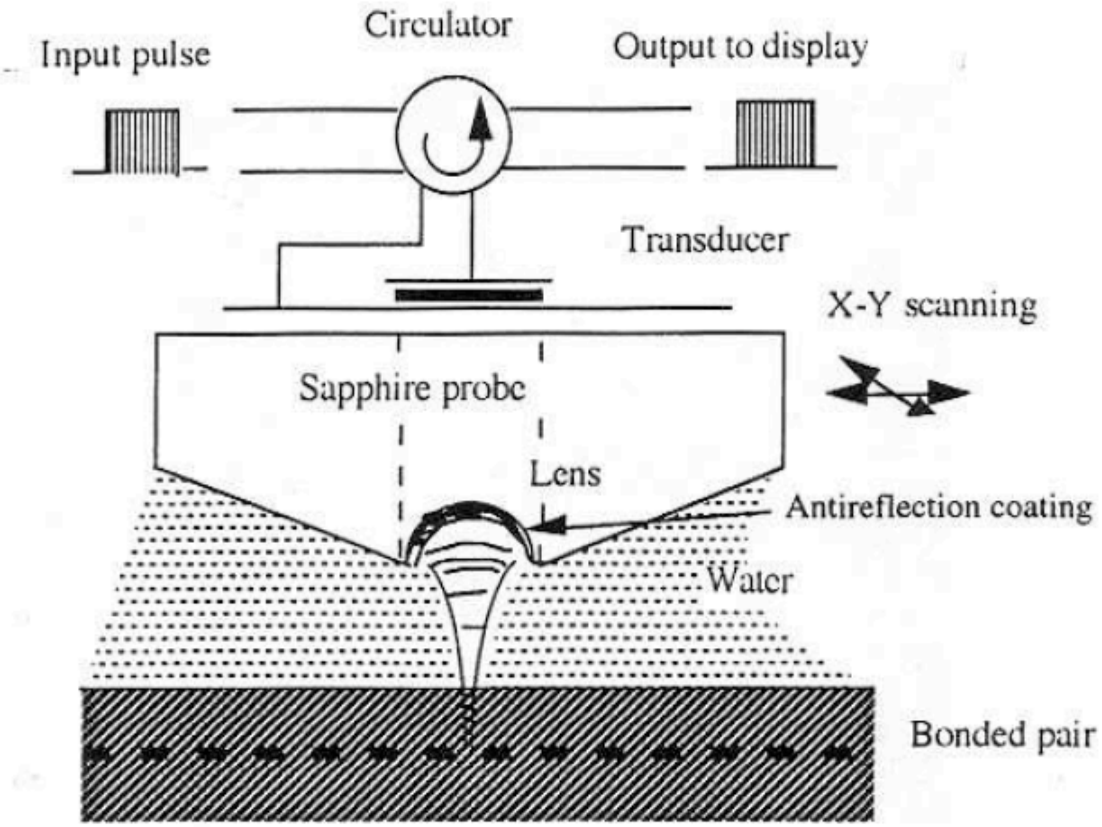
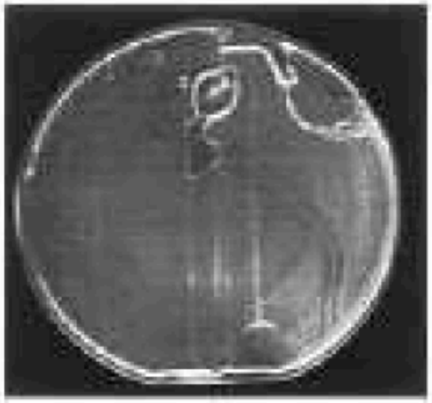


Fig. 3.5 Schematic configuration of a scanning acoustic microscope as used in the reflection mode.

Comparison of inspection techniques



(a)

X-ray topograph

(b)

Ultrasonic image

(c)

IR Image

Acoustic image of poorly bonded pair

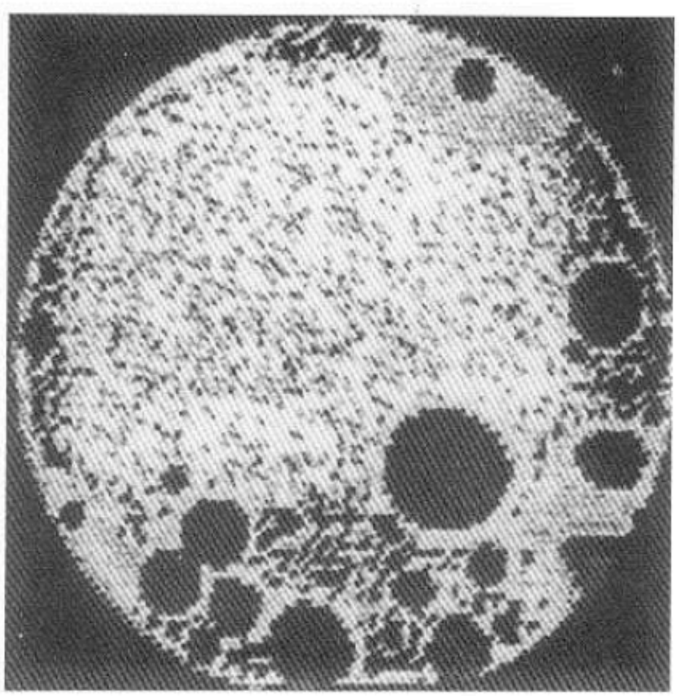


Fig. 3.6 Acoustic image of the same bonded Si/Si pair shown in Figs. 3.2 and 3.4.

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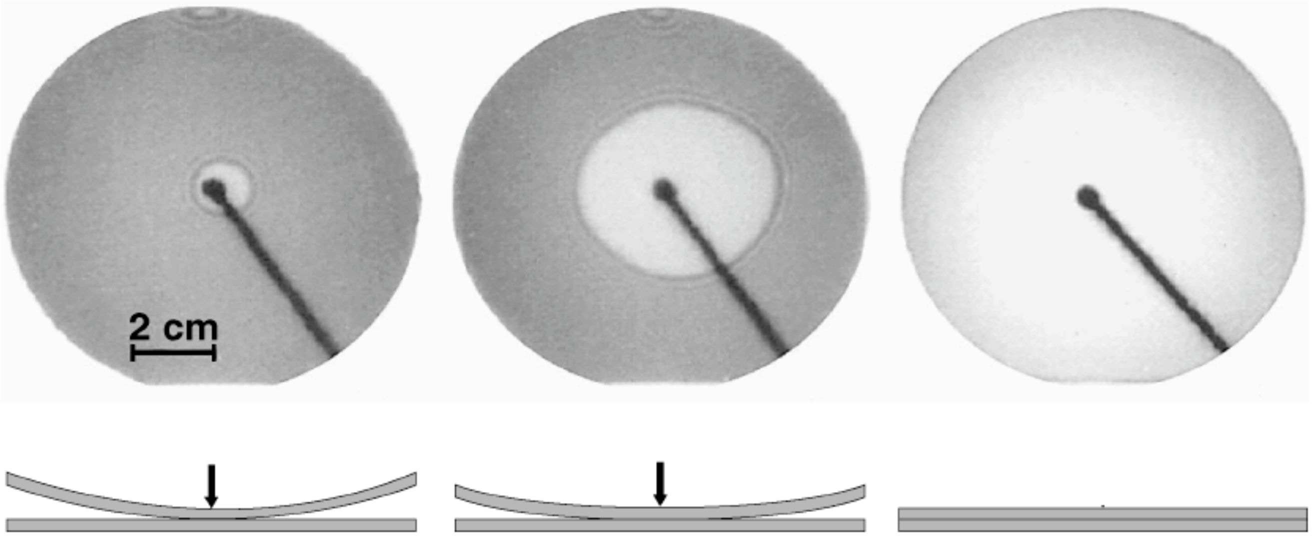
Gösele

IR Image contact bonding



- Contact initiated at center
- Intimate contact of surfaces required for subsequent bonding
  - ➢ Short range surface forces responsible for adhesion
  - ➢ Surfaces deform to achieve contact

“Hydrophilicity” of surface clean/ preparation solutions

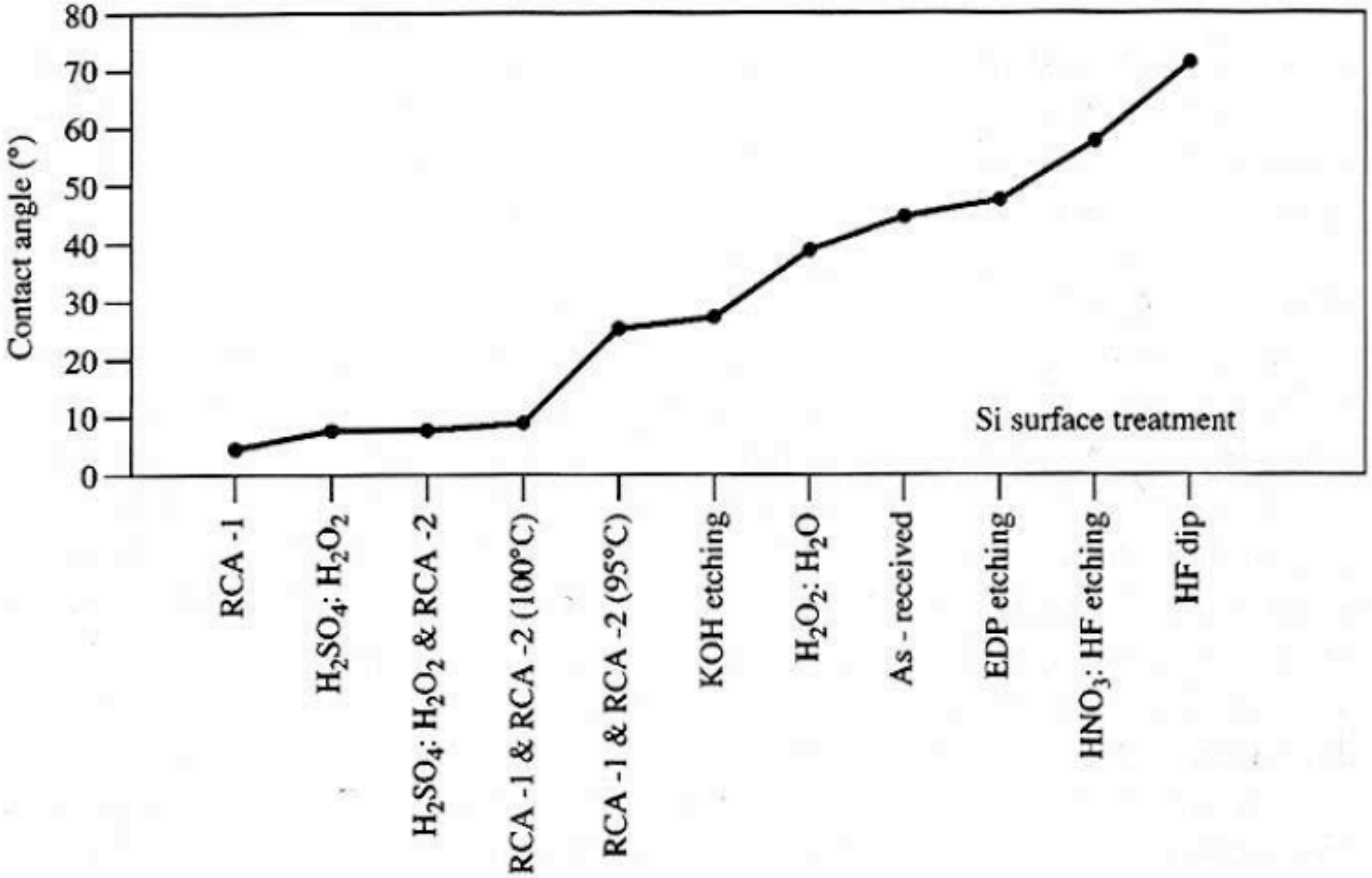


Fig. 4.7 Measured contact angle of water with Si surface prepared by various surface treatment methods.

Hydrogen bonded surface chemistry - hydrophilic

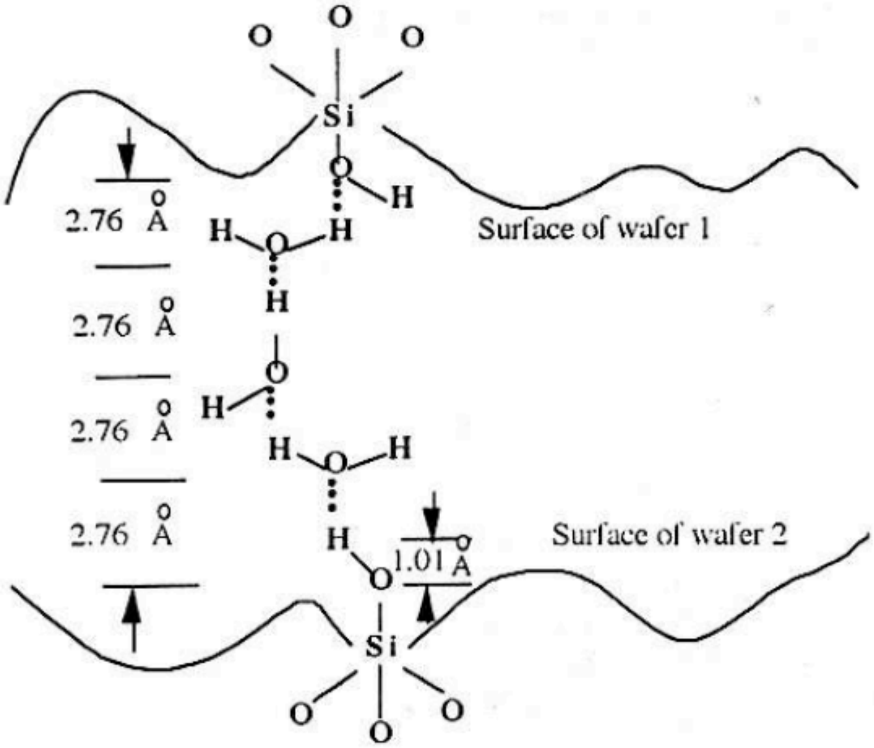


Fig. 4.3 Schematic of a linkage of three water molecules between two hydrophilic mating surfaces to bridge the wafers at RT.

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Key role played by native oxide - hydrophilic surfaces

Hydrogen bonded surface chemistry - hydrophobic

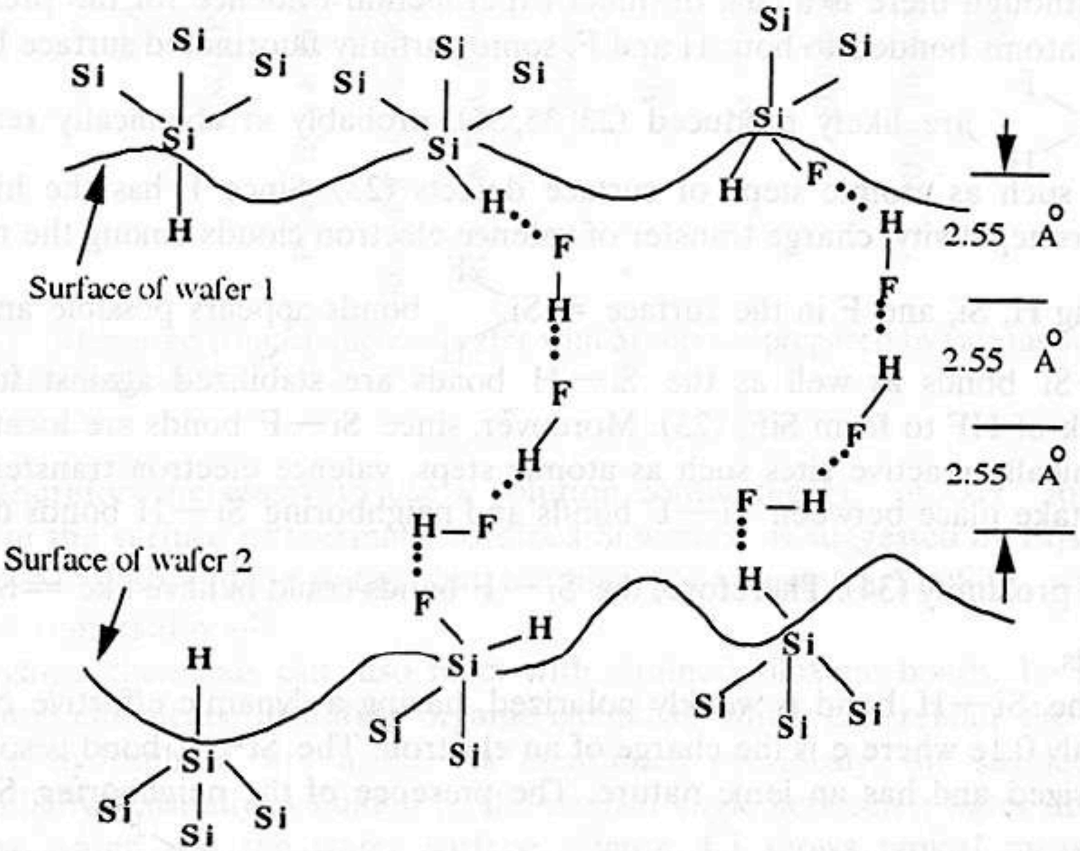

Fig. 4.8 Schematic of HF bridging across the hydrophobic bonding surfaces at room temperature.

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Typical Surface Energies

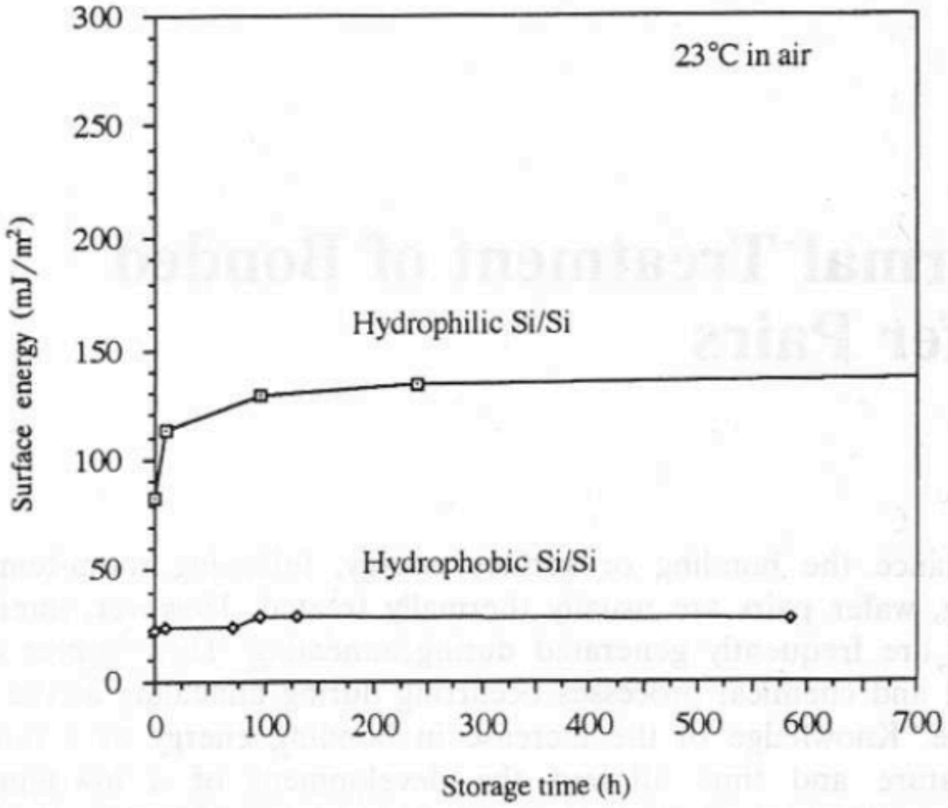

Fig. 5.1 Representative experimental results of surface energy of hydrophilic and hydrophobic Si/Si pairs as a function of storage time at room-temperature.

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and

Gösele

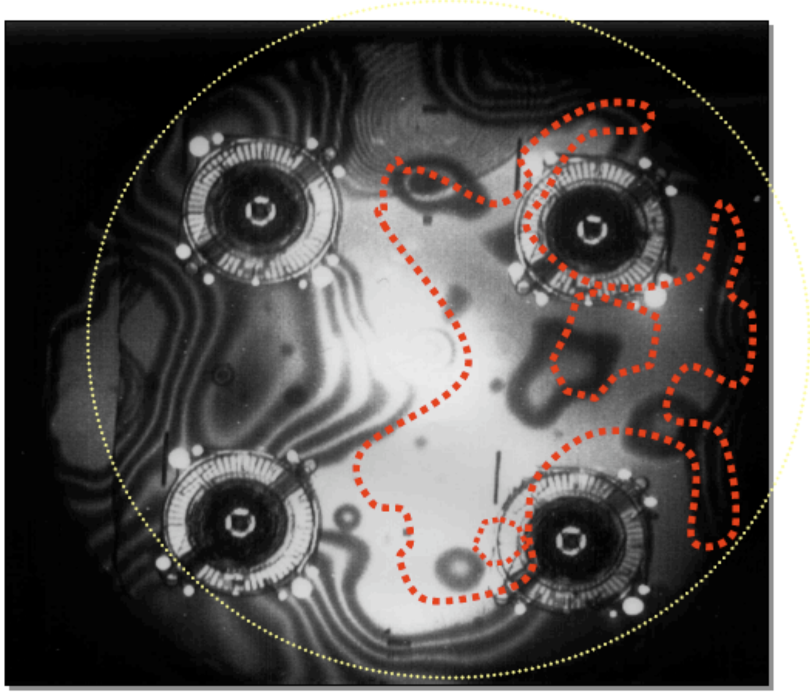
Hydrophilic energy usually greater than hydrophobic

Some effect of storage time

Surface Preparation: RCA Clean

- Developed in 1965 at Radio Corporation of America
- The industry standard for removing contaminants from wafers
- Required in most fabs prior to high temperature oxidation, difusion and deposition
- Three primary steps:
    - Organic Clean – Removal or insoluble organic contaminants with 5:1:1 H_2O:H_2O_2:NH_4OH (or H_2SO_4)
    - Oxide Strip – Removal a thin silicon dioxide layer where metallic contaminants may have accumulated as a result of (1), using diluted 50:1 H_2O:HF solution
    - Ionic Clean – Removal of ionic and heavy metal atomic contaminants using a solution of 6:1:1 H_2O: H_2O_2:HCl

Can go Wrong!



(photo courtesy MIT Microengine - N. Miki)

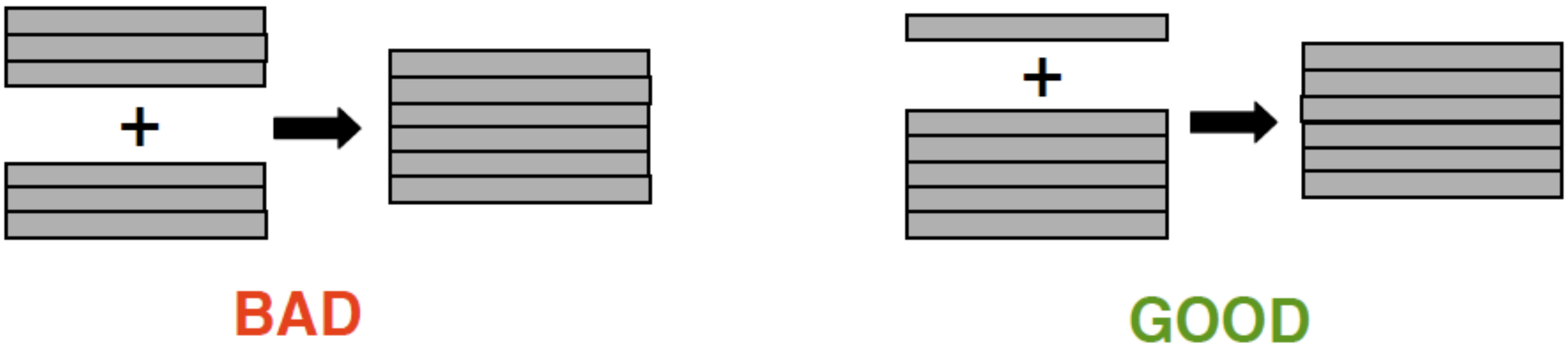
- Dark areas and fringes indicate unbonded regions
- Development of direct bonding processes requires understanding of factors that lead to unbonded regions

Wafer geometry impacts bonding

- Spontaneous wafer bonding reduces surface energy
  - Two smooth, clean, perfectly flat wafers will bond spontaneously
- When wafers are not perfectly flat, bonding requires them to bend
  - Strain energy increases
- How far will two wafers bond?
  - Wafers bond until the surface energy reduction equals the strain energy costs
- Important factors
  - Wafer thickness
  - Radius of curvature
    - Wafer bow – innate or from stressed films
    - Waviness – locally greater curvature

Wafer Geometry Impacts Bonding

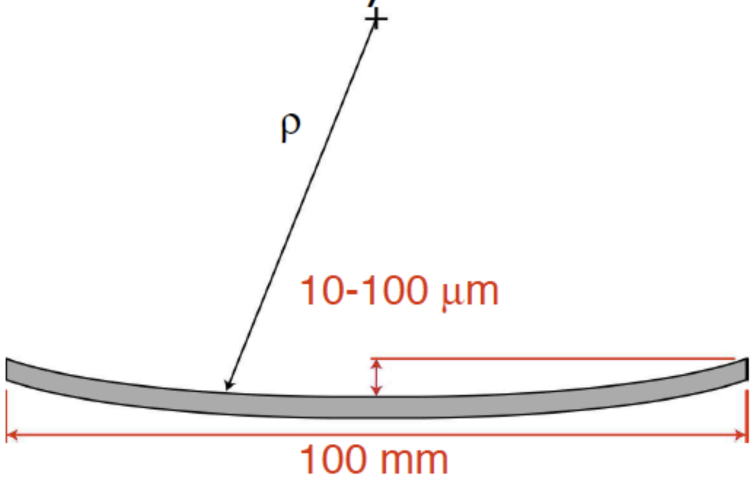
- Bonding order and strain energy
  - ➢ For given total stack thickness, the strain energy accumulates fastest for wafers of equal thickness (goes as thickness cubed)
  - ➢ To bond n wafers, add them one at a time



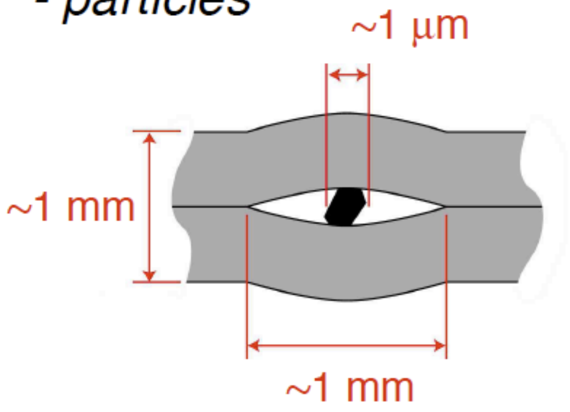
- Etched features
  - ➢ Shallow etch hinders bonding (less interaction area)
  - ➢ Deep etch aids bonding (less stiffness)

Bonding Defects

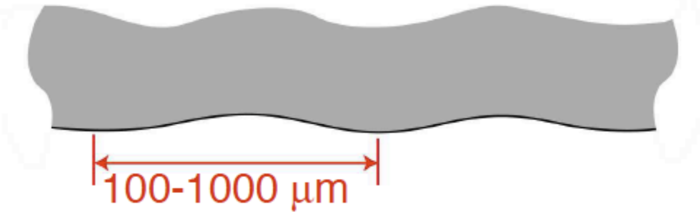
- excessive wafer bow, < 50 µm on 500 µm wafer



- particles



- surface waviness/roughness < 5nm required



- low energy surfaces - incorrect surface preparation

Key Attributes of Direct Bonding

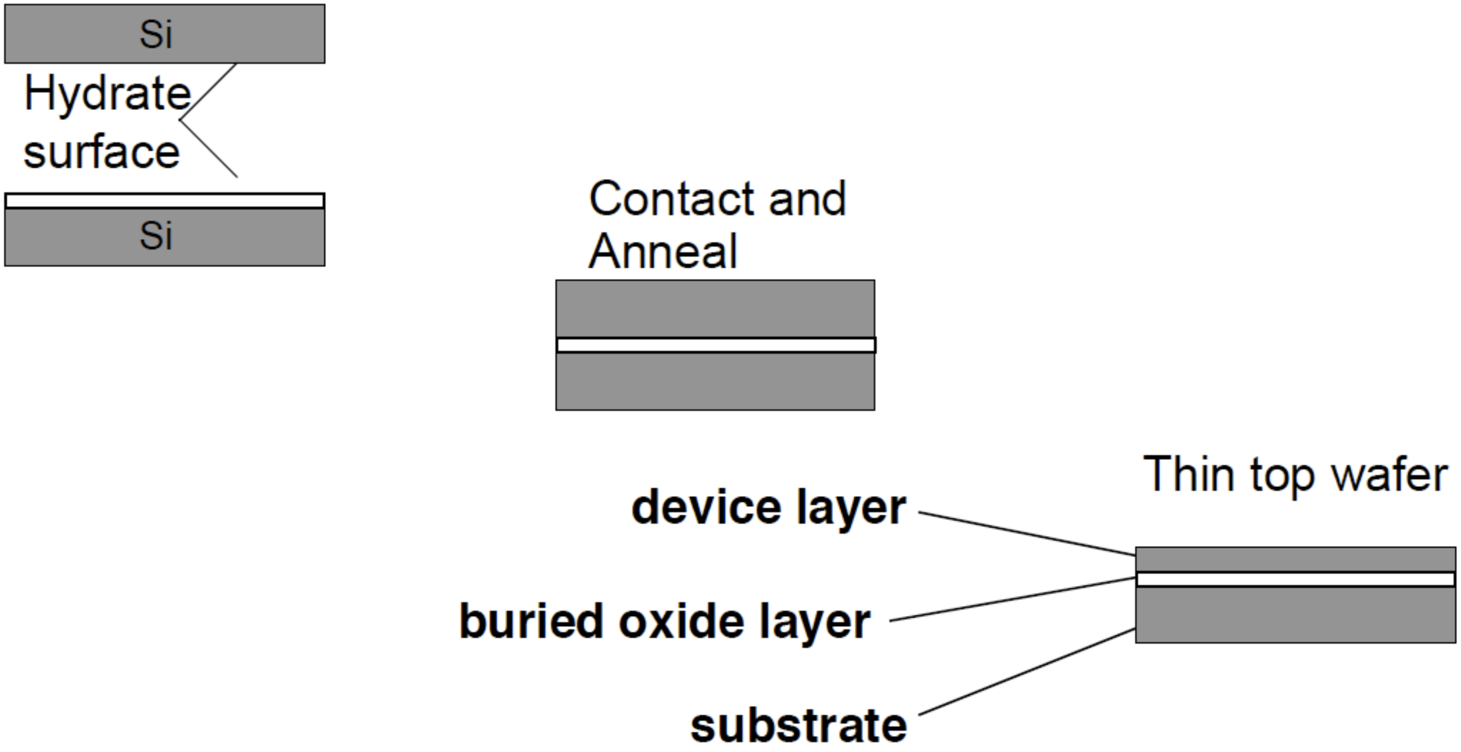
- Ability to inspect in IR
- Ability to debond and rebond in IR
- Bond toughness/strength approaches that of Si after annealing
- For Si-Si wafer bonds no thermal mismatch – important for sensitive instruments
- High temperature technique, allows high temperature operation
  - But must come early in temperature hierarchy of processing
- Relatively defect sensitive, particularly in intitial contacting stage
  - Particles, roughness, bow

Wafer bonding and yield

- Yield in MEMS can require a whole-wafer outlook, unlike IC processing
- A micon-scale defect can create a mm- to cm-scale defect
  - ➢ Amplification by wafer stiffness
- Can have a die yield of 100% on individual wafers and not get any devices if defects outside the die area prevent wafer bonding
- Cleanliness (particulates, organics) is critical to prevent defects; organics can outgas on anneal
- Adjust process to minimize stiffness in bonding
  - ➢ At least one of the wafers should be thin (and therefore relatively pliable) when going into the bonding process

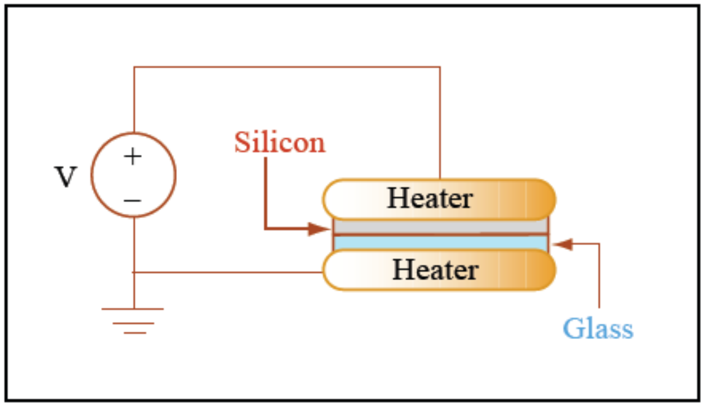
Silicon-on-insulator

- Bonding to oxidized wafers is also possible, leading to silicon-on-insulator wafers



Anodic Bonding

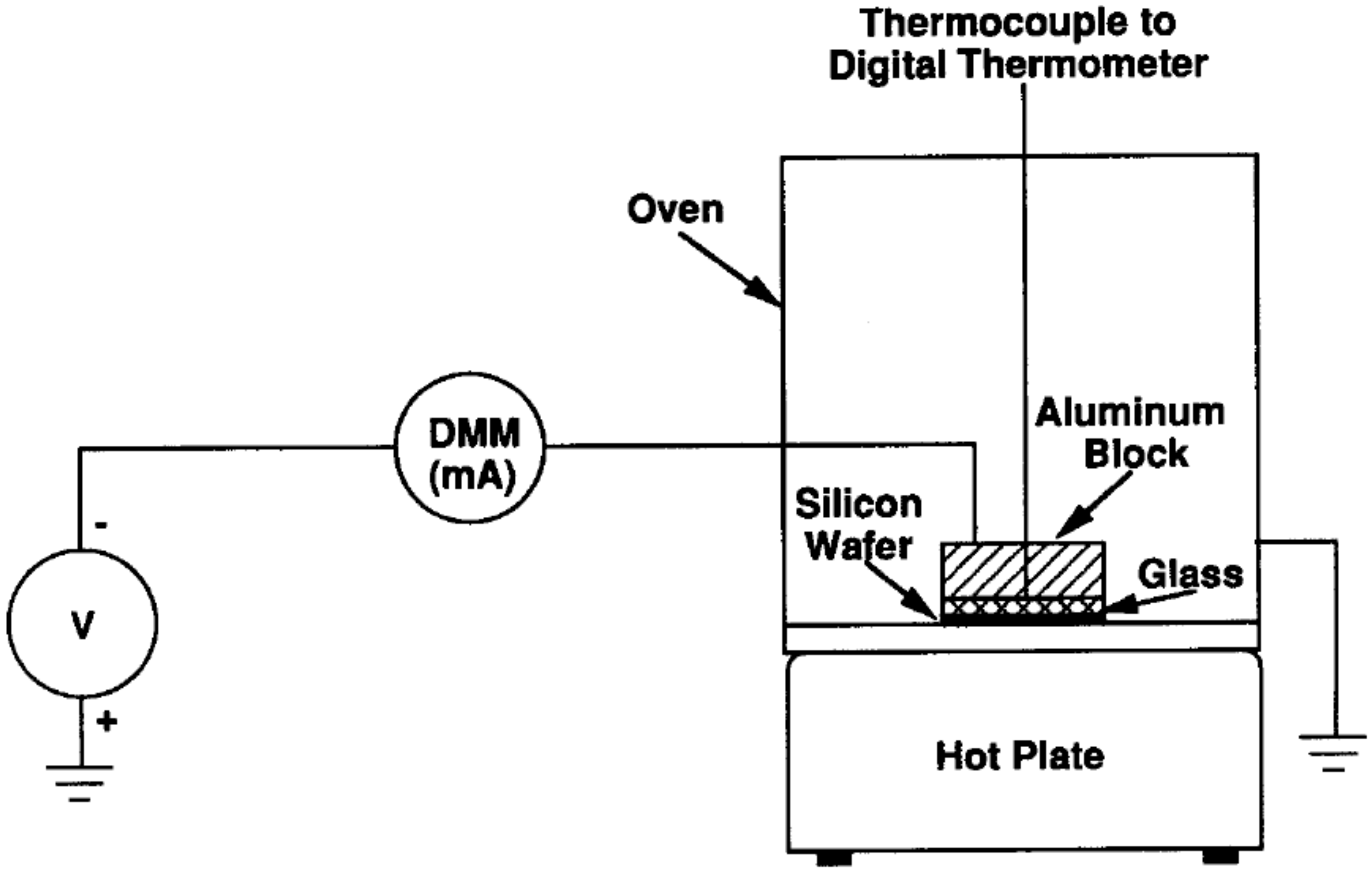
- The mobility of sodium ions in the glass drives anodic bonding
- The wafers are heated to temperatures of about 500C; a positive voltage (300V – 700V) applied to the Si repels sodium ions from the glass surface
- Suspectible to particulates, but less so than direct bonding
- Commonly used as a packaging step



Anodic Bonding for Si:Glass

- Initial interface contact, then apply temperature and voltage (Si connect to anode and glass cathode)
- Applied temperature allows Na+ cations in glass to move to negative charged cathode
- Na cations leave a negatively charged depletion region near interface, and an electrostatic field generates an attractive force between the surfaces that pulls them together
- Electrostatic pressure causes creep deformation which flattens the gaps along the interface for uniform contact
- Simultaneously, SiO_2 bonds forms once two surfaces are in contact

Anodic Bonding Apparatus



Anodic bonding: process parameters

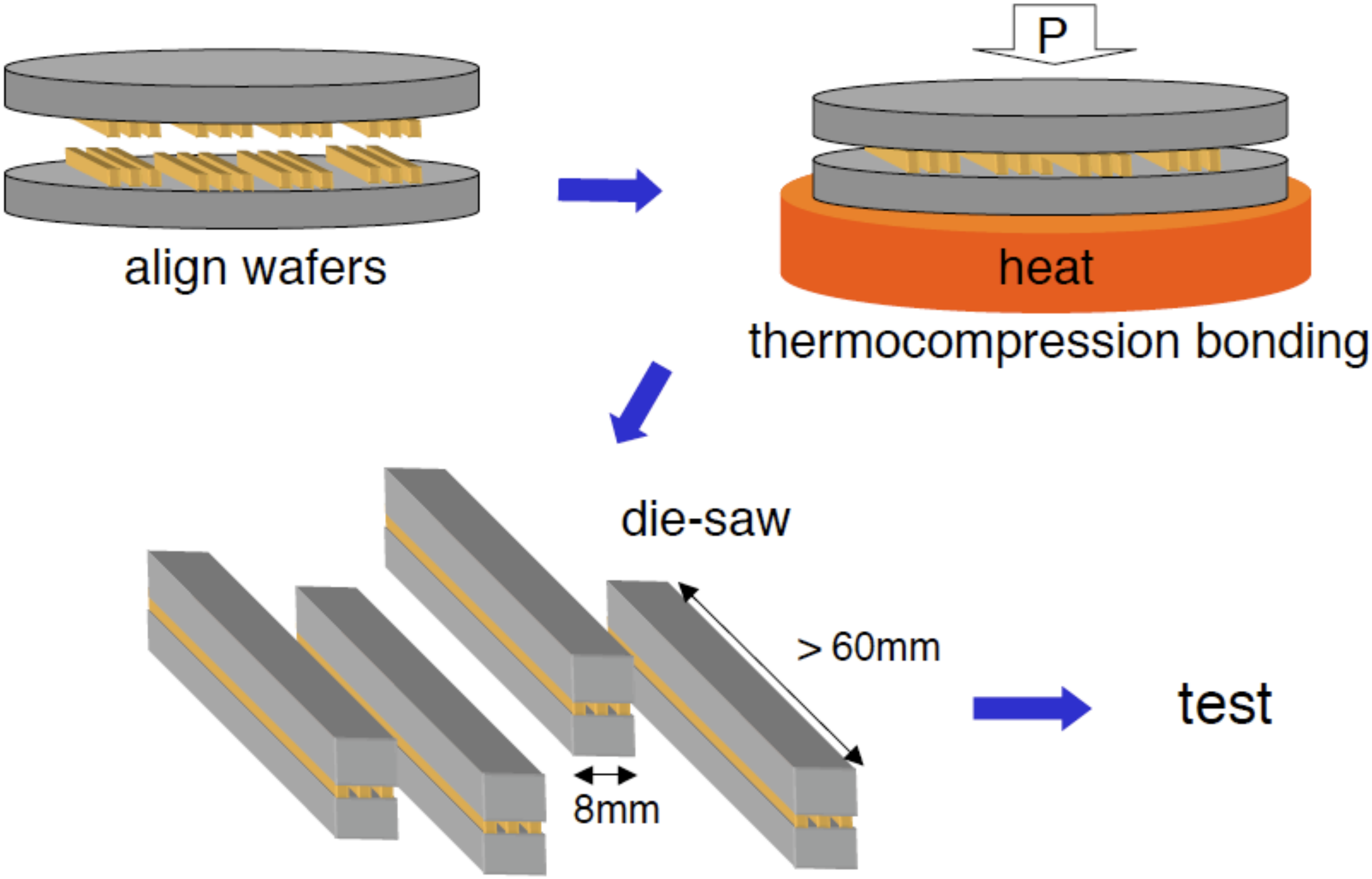
- Process parameters involved
  - Applied voltage (500-1000V)
  - Bonding temperature (200-500 C)
  - Thickness of glass, and pretreatment of surface all influence bond strength and bond time (~ 10 min.)
- Requires close CTE match between glass and Si (Pyrex 7740 – Borosilicate glass often used)
- Less sensitive to surface roughness vs. silicon direct bonding
- For wafer level, careful electrode deisgn required
- Hermetic seal results

Thermocompression Bonding

- Either use of interlayer material or between bulk substrates
- Simultaneous application of pressure and temperature during bonding
  - ➢ Usually referred to as diffusion bonding at macroscale (e.g. DB titanium for gas turbine compressor blades)
- Pressure deforms the interlayer surface
  - ➢ Increase mass transport at surface
  - ➢ Lower temperature than pressure-less direct bonding

Gold Thermocompression

(test specimens - but could be devices)



align wafers

thermocompression bonding

die-saw

test

Solder Bonding

- Uses Solder as an intermediary; ready electrical connection
- Solder melts in order to form bond, surfaces must allow wetting
- More relaxed on particulate and surface roughness requirements than anodic or direct bonding
- Low temperature process (100-600 c)
- Components oxidizes easily → prevets proper wetting of solder w/substrates (reducing atmpspheres, fluxes)
- Often die-level process rather than wafer level
- Issues with voids, trapped gases, fillets at edges

Glass Frit bonding

- Similar in attributes to solder bonding
- Glasses soften – lower viscosity rather than melting
- A frit is a fine powder that can be applied as an ink or a paste, and patterned, e.g. by screen printing
- Glass flows and wets surfaces – wets to oxides well
  - Usually pressureless, but force can be applied
- Flow temperatures 300C → 1100 C tailor by glass composition
- Can tailor glass composition to minimize CTE mismatch
- Moderately sensitive to processing conditions, voids, wetting
- Relatively insensitive to surface roughness, particles
- Can use as seals around pin outs, fluidic interconnects

Designing process flows for cleanliness

- If you are planning to do a fusion bond, design your process flow to prevent exposure of boding surfaces to junk
  - Cleanliness is a good idea for anodic bonding, too, but anodic bonding is less pricky
- Some junk washes off easily, but some doesn't
- Example: deep reactive ion etching's passivation layer is reluctant to come off (ashing helps somewhat but isn't perfect)
- Work around: if possible, start your process by coating your wafer with a protective layer, like oxide. When you remove it right before bonding, it carries the junk away from it

Pressure Sensor

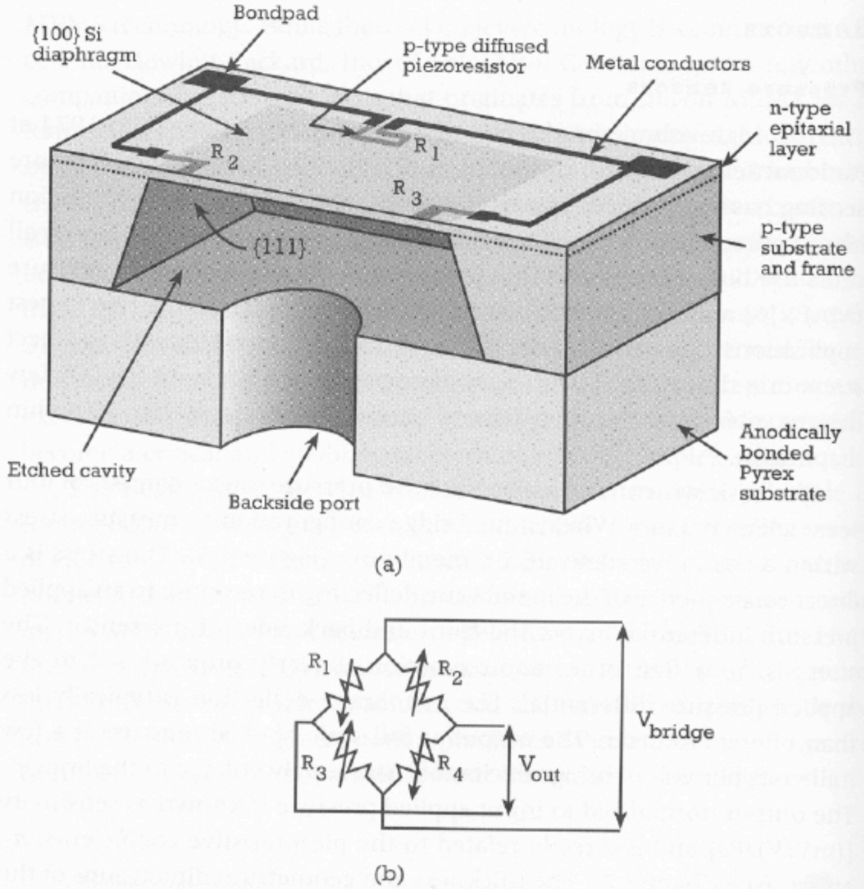


Figure 4.5 (a) Schematic illustration of a pressure sensor with diffused piezoresistive sense elements. (b) The four sense elements form a Wheatstone bridge configuration.

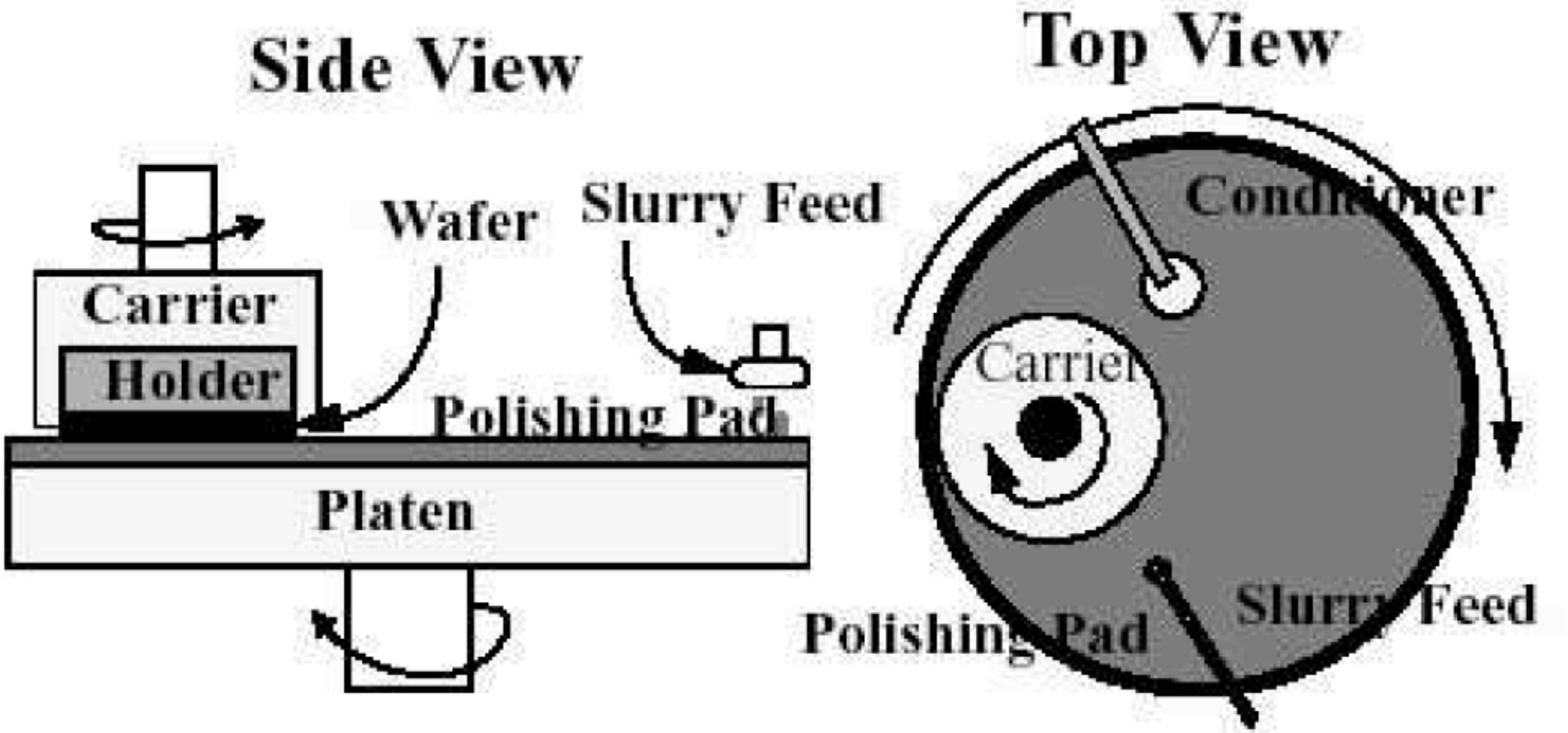
Wafer Bonding Conclusions

- Wafer bonding is a key technology for MEMS, packaging and mainstream IC microelectronics
- Variety of bonding technologies available
  - ➢ Direct bonding, anodic bonding, thermocompression, braze/ soldering, glass frit bonding (and polymeric bonds)
- Technologies are complementary
  - ➢ Hierarchy of temperatures (lower temp later in process)
  - ➢ Sensitivity to different process parameters – surfaces, particles, wafer curvature, die level vs. wafer level
- In most cases reasonable understanding and control of processes has been achieved

Chemical Mechanical Polishing (CMP)

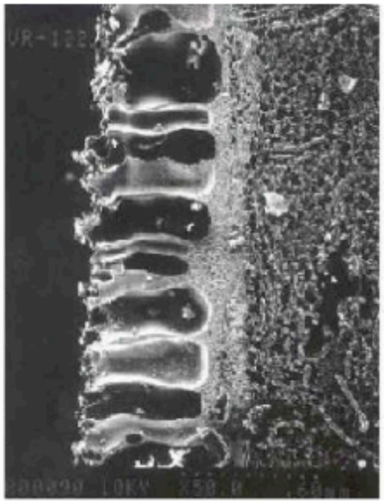
- Often used to planarize interlayer dielectric insulators
- Typical surface roughness less than 1 nm, but waviness can be much bigger
- Combination of mechanical polishing and chemical etching
- Using an abrasive slurry dispersed in an alkaline solution
- High, narrow features polish faster than low, uniform features

CMP


Side View
Top View
Wafer
Slurry Feed
Carrier
Holder
Polishing Pad
Platen
Conditioner
Carrier
Slurry Feed
Polishing Pad

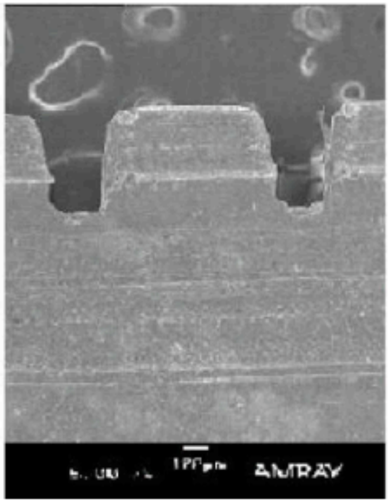
Pad Types

Impregnated felts



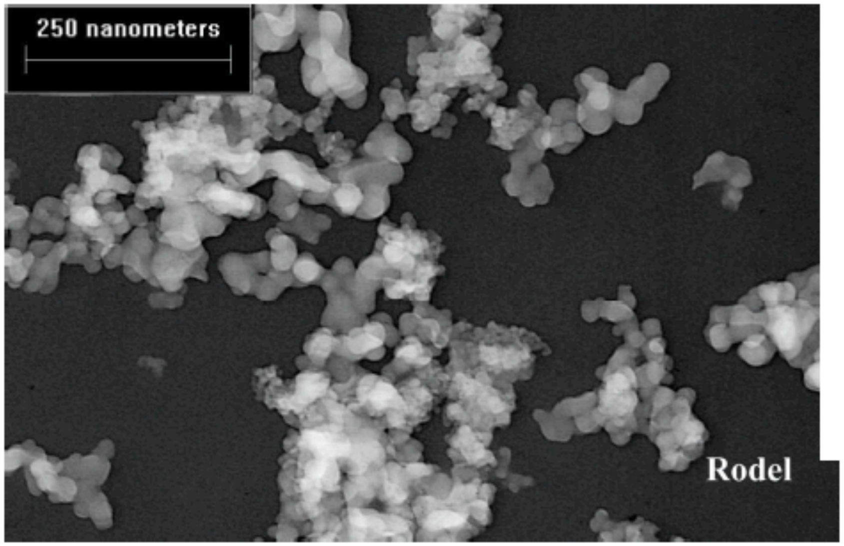
Poromerics

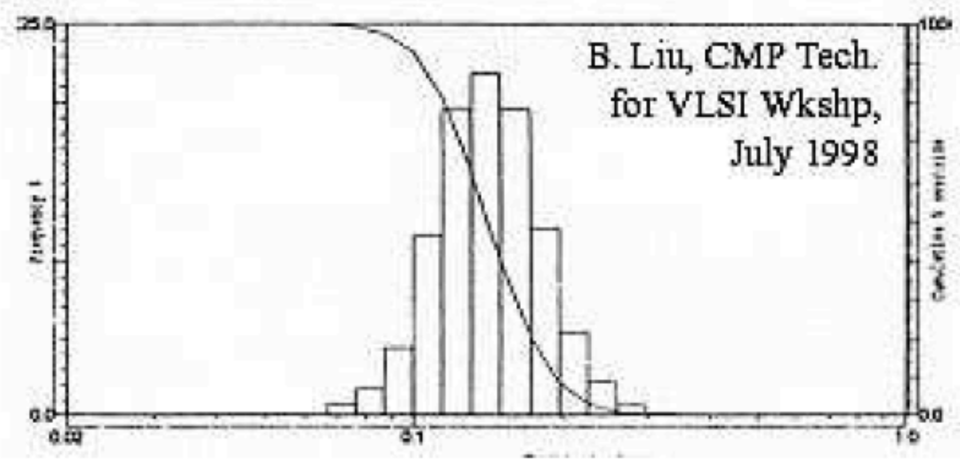
Filled polymer



Unfilled polymer

Slurry Parameters



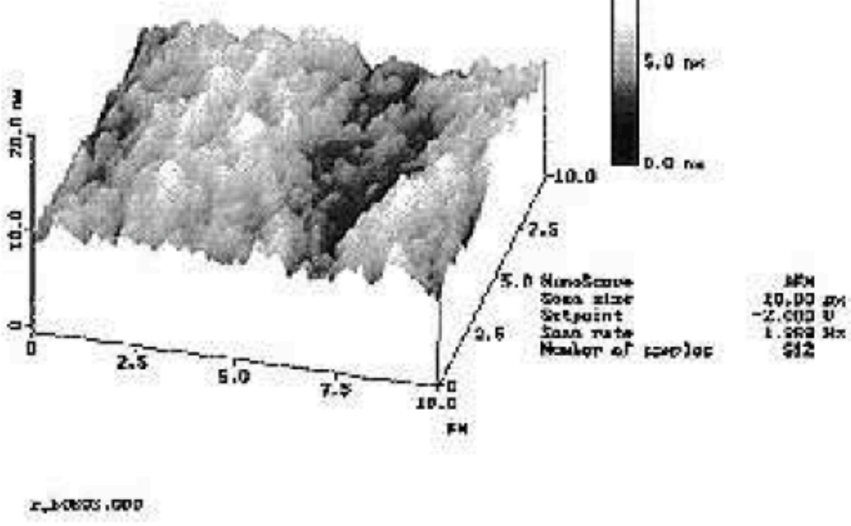


B. Liu, CMP Tech. for VLSI Wkshp, July 1998

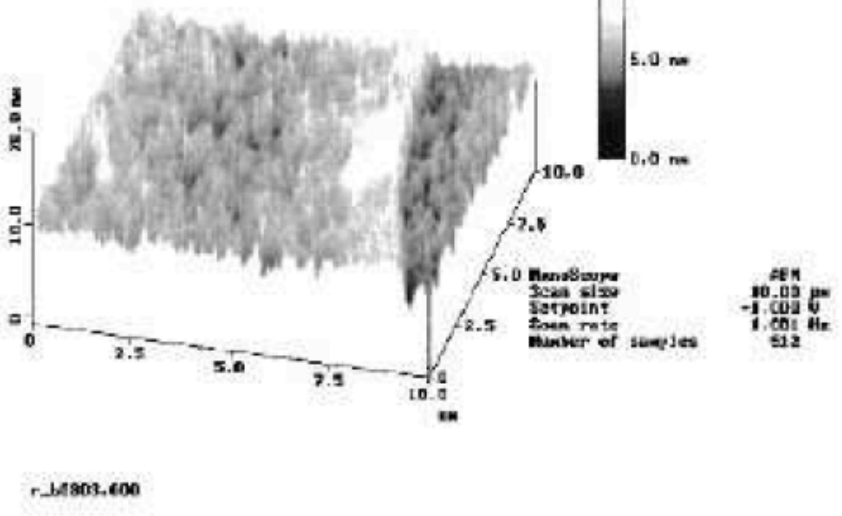
- Colloidal or fumed particles suspended in solution
    - For ceramics, dielectrics, silica, ceria in alkaline solution
    - Metals, silica, alumina in variety of solutions
- Particle sizes in 50 nm – 1um range – morphology, tendency to agglomerate (leads to scratching)
- Complex chemistry – need to optimize and control
    - Removal rates, selectivity (undesirable), damage, corrosion

Surface Morphology

C. Gui et al., *J. App. Phys.*, 85(10), 1999.

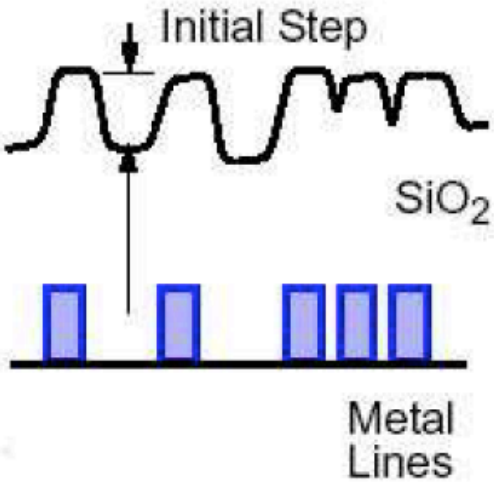


CMP

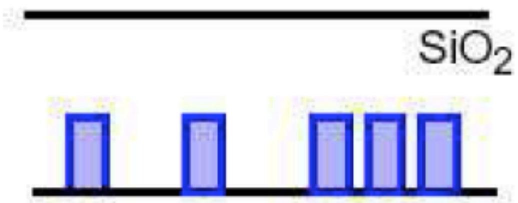


HF/KOH Etch

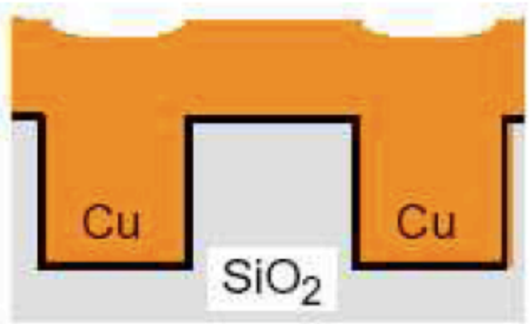
CMP in microelectronics

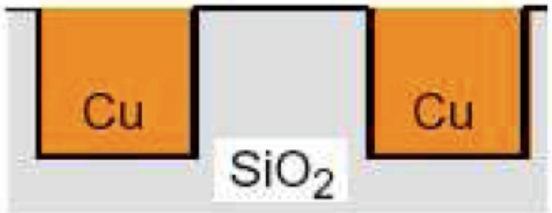


Planarizing to surface



Removing overburden





CMP in MEMS

- Surface micromachining
  - ➢ Typically < 5 um poly and oxide films
    - CMP to reduce topography
    - Polish-back for embedded films enables new structures
    - Film/surface roughness control using CMP
- Bulk micromachining (wet etch/DRIE) and wafer bonding
  - ➢ Processing 200-500 um thick wafers: cavities, membranes, holes
  - ➢ Multiple wafers bonded in stack
    - Good bonding may require control of surface finish via polishing
- LIGA
  - ➢ Extremely high aspect ration, metal/plated parts
    - Polish-back to free/release parts from mold