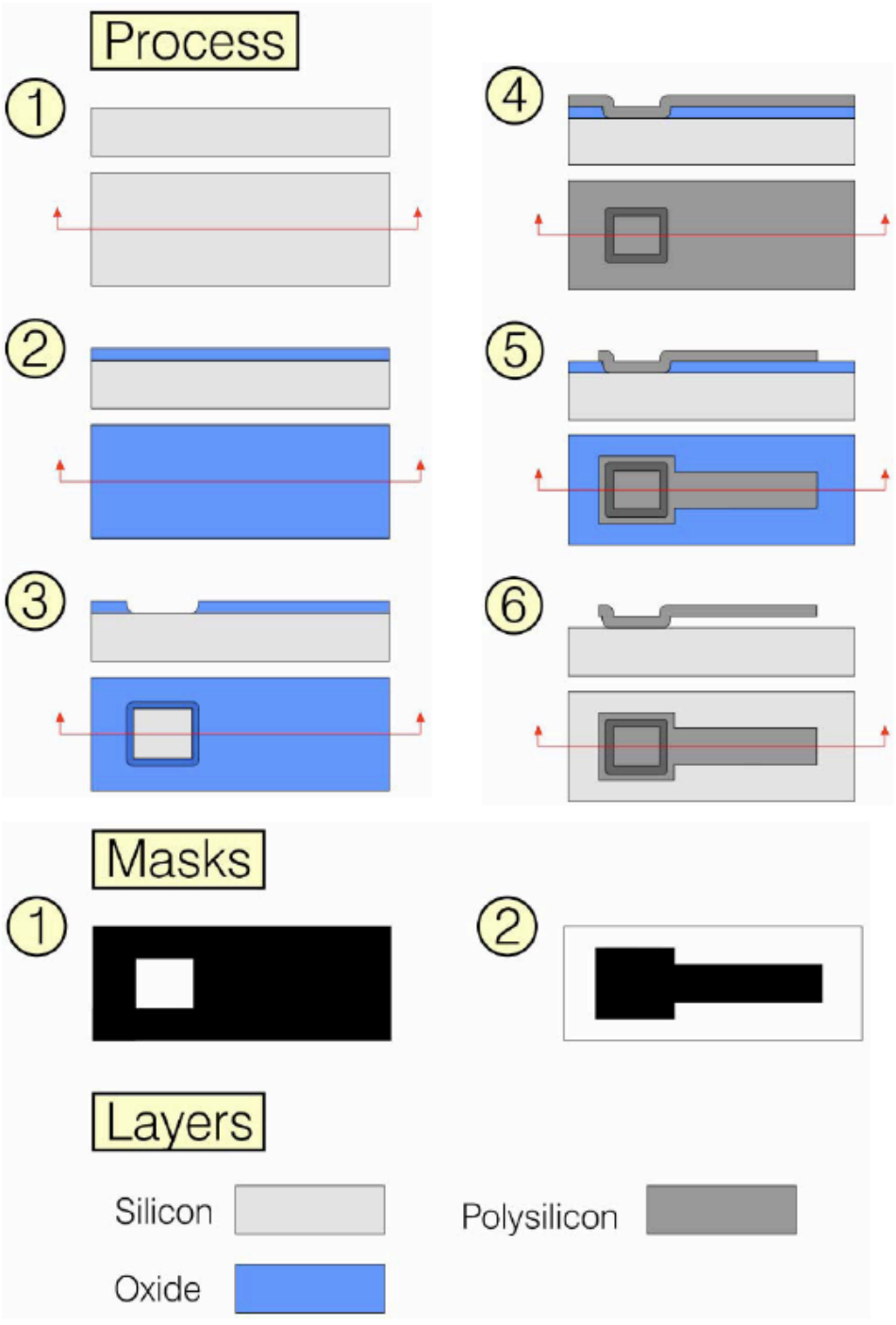
HW #1 Solutions

Problem #1:

Proposed process step	Error
1. Start with a silicon wafer	
2. Deposit 1 μm of polysilicon	Must precede with RCA clean. Also, must have some layer (such as oxide or nitride) separating poly from substrate to serve as a "stop" layer during etching.
3. Perform photolithography using positive photoresist (not shown) and wet-etch the polySi using KOH.	Can't perform KOH etch when PR mask is used; PR will lift off immediately. Also, this step must be followed by PR removal .
4. Thermally grow 1 μm of thermal oxide	Can't grow thermal oxide on polysilion; the oxide will eat much of the polysilicon and the surface will not be planar since the oxide will grow much slower in-between the poly plates. Deposit oxide instead. Also, must precede with RCA clean of wafer.
5. Perform photolithography using positive photoresist (not shown) and wet etch the oxide in 49% HF.	Can't use 49% HF with PR as a mask; the PR will lift off. Use BOE instead. Also, this step must be followed by PR removal. Also, we won't get perfect alignment between the oxide opening and right edge of poly 1.
6. Deposit 1 μm of polysilicon.	A wafer clean such as Piranha should precede this deposition to ensure a quality deposition.
7. Perform photolithography using positive photoresist (not shown) and dry etch the polysilicon using SF_6 plasma.	SF_6 leads to isotropic etching and undercutting, which might or might not be an issue depending on the dimensions of the cantilever. Also, we won't get perfect alignment between the left edge of poly level 2 and the left edge of oxide cutout. Also, this step must be followed by PR removal.
8. Release the cantilever by etching the oxide with 49% HF	Must be followed by some drying process, as wet etching alone will lead to stiction problems.

Simpler Process:

1. **Start with a silicon wafer, perform RCA clean with HF dip.**
2. **PECVD 1 μm of sacrificial oxide.**
3. **Perform photolithography using positive photoresist (not shown) and Mask 1; then wet-etch the oxide using BOE. Then ash resist and perform RCA clean (without HF dip).**
4. **LPCVD 1 μm of polysilicon.**
5. **Perform photolithography using positive photoresist (not shown) and Mask 2; then dry-etch the polysilicon using reactive-ion etching. Then ash resist and perform RCA clean (without HF dip).**


Process
1
2
3
4
5
6
Masks
1
2
Layers
Silicon
Polysilicon
Oxide

Problem #2:

a) Some challenges:

1. Order of depositions: the polysilicon must go down before the metal because of thermal compatibility (poly deposition is carried at a high temperature)

2. Because of topography concerns, you have to pattern the films on the cantilever before you etch the hole beneath it. This requirement makes the organization of the process flow a bit more challenging and involved. Additionally, the cantilever, once released, won't be robust enough to tolerate lithography.

4. A wet etch like KOH would undercut the cantilever effectively, but you can't mask it with resist. You must know what materials will effectively mask the wet etch. A lack of consideration here can cause inadvertent damage to structural/functional parts of the device.

5. How do you define a cantilever that is precisely 1.5 microns thick? You will need to incorporate a thickness-determining layer into the structure of the wafer.

b) Three approaches:

1. Use an SOI wafer to set the thickness of the cantilever. Deposit LPCVD nitride to provide electrical isolation between the cantilever and the polySi heater. Deposit polySi for the heater, dope it, then perform photolithography and dry etch the poly, stopping on nitride, defining heater pattern. Strip the resist, clean the wafer, and deposit LPCVD nitride everywhere to isolate the heater from metal layer. Deposit aluminum, perform photolithography, and etch it into the correct shape. Use thin resist photolithography to mask around the etch hole. Dry etch the nitride to expose the silicon and open contact pads, then define the contour of the cantilever by dry etching to the buried oxide. (*) Use BOE to remove the exposed oxide. Flip the wafer over, and dry etch several times to strip blanket films from the back (nitride, then poly, then nitride). Pattern the back with thick photoresist, then DRIE through to define cantilever.

2. This option is very similar to the preceding sequence, but it omits the final DRIE step. Follow the process to point (*). Repattern so that the resist sticks out a little beyond the cantilever edges, and dry etch the exposed buried oxide. Strip resist and recoat, patterning so that the resist extends beyond the cantilever's Si, covering it entirely (very important.) Use a XeF_2 isotropic dry etch to undercut the cantilever; the cantilever itself is protected by resist and oxide, while the Si underneath gets removed.

3. This listing is the approach we will use in part c. Briefly: Grow doped, KOH resistant Si by epitaxy, deposit nitride, followed by polysilicon. Dope the poly and then pattern it. Deposit another layer of nitride and then pattern it to open contact pads. Deposit a Ti-Au bilayer and use liftoff to define the metal layer. Dry etch the nitride and the epitaxial silicon to define the cantilever. KOH etch the substrate to release it. See part c.

c) Using the third approach from above[1], we detail the process flow here. Key device cross sections, planar views, and the mask set are shown in Figures 2-4. Note that the cross section taken (A-A') is not straight but rather bent around a corner to show the different critical parts of the device during the fabrication process.

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[1] adapted from: Riethmuller and Benecke, "Thermally Excited Silicon Microactuators," *IEEE Transactions on Electron Devices*, Vol 35, No. 6. June 1988.

Step		Description
Starting Material: Silicon wafer		4" or 6"; (100) orientation; 500 μm or 650 μm thick
1	**Clean**	Standard RCA.
2	**Deposit p^+ Si**	Using epitaxy, thickness = 1.5 μm. Heavily doped Si (example: Boron concentration ~ 1.3×10^{20} cm^{-3}) is KOH resistant.
3	**Deposit nitride**	LPCVD, thickness = 0.1μm. Used to electrically insulate the heater from the p^+ Si. Will cover both sides of wafer.
4	**Deposit polysilicon**	LPCVD, thickness = 0.5 μm. Will act as the heater. Also covers both sides.
5	**Deposit oxide**	LPCVD, thickness = 0.2 μm. Will act as a protective shield to poly during the ion implantation step. Also covers both sides
6	**Dope polysilicon and anneal**	Using ion implantation of Boron. Follow with annealing (at ~1000°C) to activate the implant.
7	**Etch oxide**	BOE for ~ 2 minutes.
8	**Photolithography**	Spin cast 1 μm thick positive photoresist, prebake; expose MASK 1, develop, postbake. Mask 1 defines the shape of the polysilicon heater.
9	**Dry etch polysilicon**	Using HBr for example (used by AME5000 in MTL-ICL). HBr etches poly anisotropically. The heater is now patterned.
10	**Strip PR**	By ashing for example.
11	**Clean**	Standard RCA.
12	**Deposit nitride**	LPCVD, thickness = 0.1 μm. Used to electrically insulate the heater from the metal layer to be deposited next. Will cover both sides of wafer.
13	**Photolithography**	Spin cast 1 μm thick positive photoresist, prebake; expose MASK 2, develop, postbake. Mask 2 is used to open contact pads to the poly heater.
14	**Dry etch nitride**	Using CHF_3/O_2 plasma for example . This patterns the contact pads into the heater.
15	**Strip resist**	By ashing, for example
16	**Photolithography**	Using image reversal resist and MASK 3. Thickness of resist about 2 μm (3 times that of the layer to be lifted off, plus an extra 0.5 μm to counter the step coverage problem due to the presence of the 0.6 μm poly-nitride step). Image reversal (negative) resist necessary for lift off process later on.
17	**Deposit Ti-Au bilayer**	E-beam evaporation (good for lift-off). Thickness of titanium ~ 100 Å, thickness of gold ~ 0.5 μm. Ti used as adhesion layer.
18	**Lift-off Ti-Au bilayer**	Acetone. Follow by water rinse. Now the metal layer is patterned.
19	**Clean**	Using Nanostrip
20	**Photolithography**	Spin cast 1 μm thick positive photoresist, prebake; expose MASK 4, develop, postbake. Mask 4 defines the shape of the cantilever.
21	**Dry etch nitride**	Using CHF_3/O_2 plasma for example.
22	**Dry etch epitaxial Si**	Using HBr, for example.
23	**Strip resist**	By ashing, for example.
24	**Etch silicon (from top)**	Using KOH and the top (patterned) and bottom nitride layers and metal layer above the contact pads as masks. Etch 30 μm deep (etch rate and hence timing for this step depend on the KOH temperature and concentration). Since convex corners become undercut, the cantilever will be released. We are making the hole deeper then required to make sure that the cantilever doesn't stick to its bottom because of the wet etch.

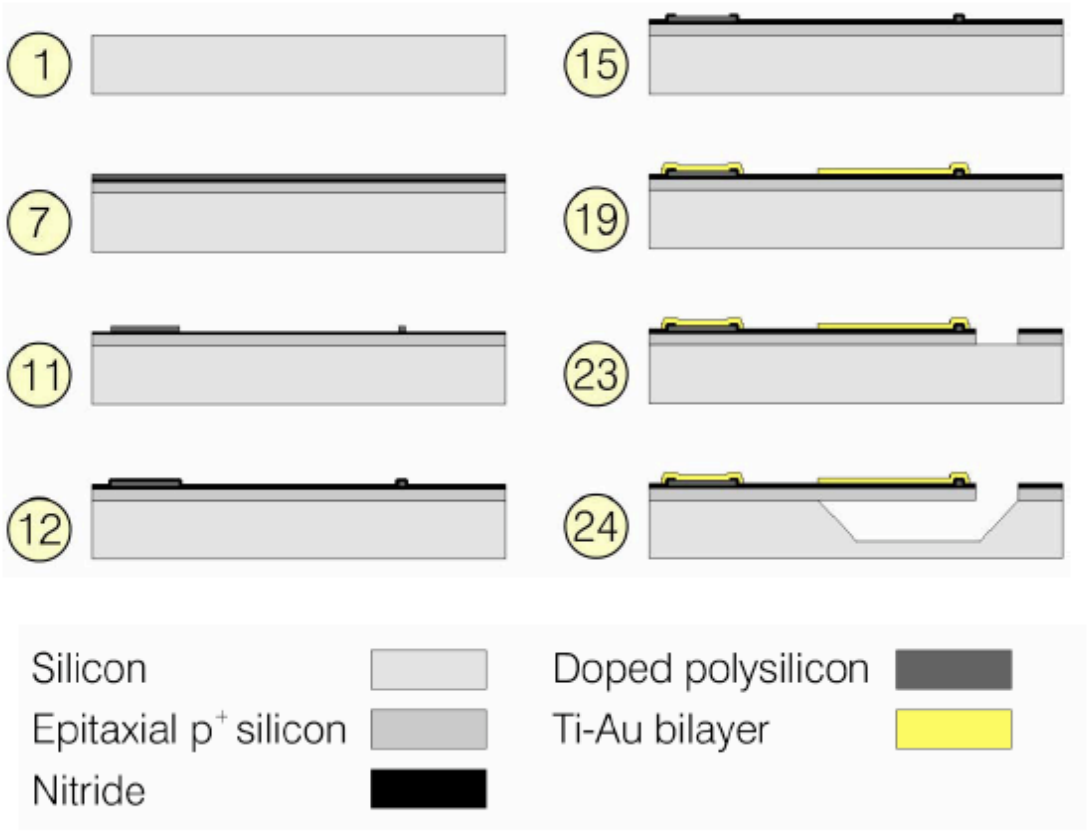


Figure 2: Important cross-sectional views

Note: Some films are deposited on the back side of the wafer. Those films are not explicitly shown in these cross sections simply because the process flow does not mandate any backside processing. Not including such films aims to minimize the "clutter" in this figure.

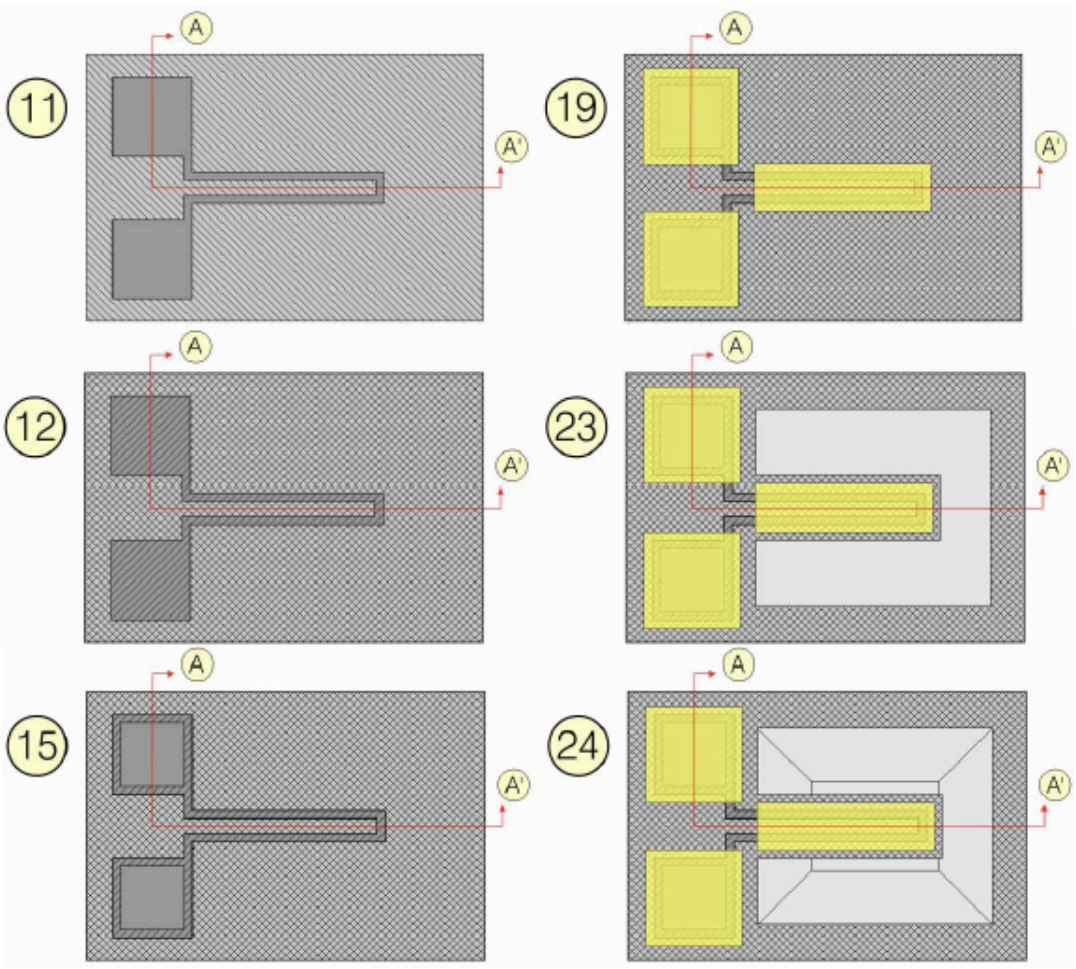
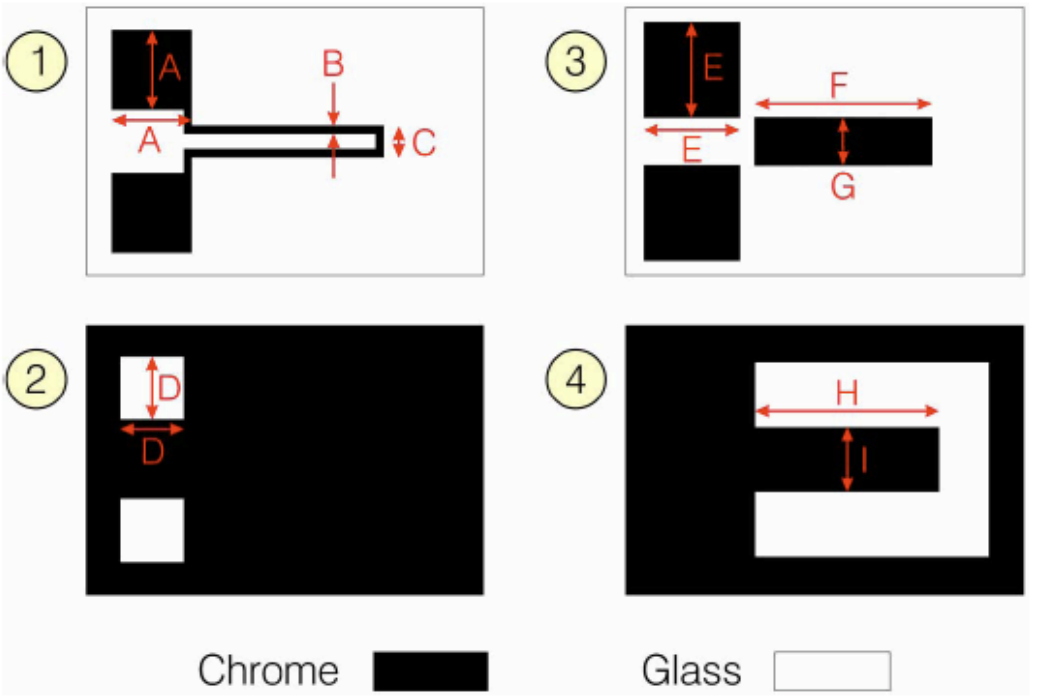


Figure 3: Important planar views

Note: We highlight the two nitride layers using different shading in this planar view. (They are simply shown in black in the cross-sectional views.) Additionally, the Ti-Au bilayer is drawn with some degree of transparency to avoid obscuring underlying features. In reality the Ti-Au bilayer is not transparent.



A=D+2μm or more	C=16μm or so	H=100μm
E=A+2μm or more	F=98μm or so	I=20μm
B=4μm or so	G=18μm or so	

Figure 4: The mask set used for this process along with some key dimensional constraints

Note: Generally, bond pads are at least 100μm × 100μm in size. Anything smaller is difficult to bond using a wirebonder. There also has to be adequate spacing between the bondpads. Generally, anything less than 100 μm is considered "risky". The bondpads are not drawn to scale in this process flow. If they were drawn accurately, it would be difficult to see the features on the cantilever.